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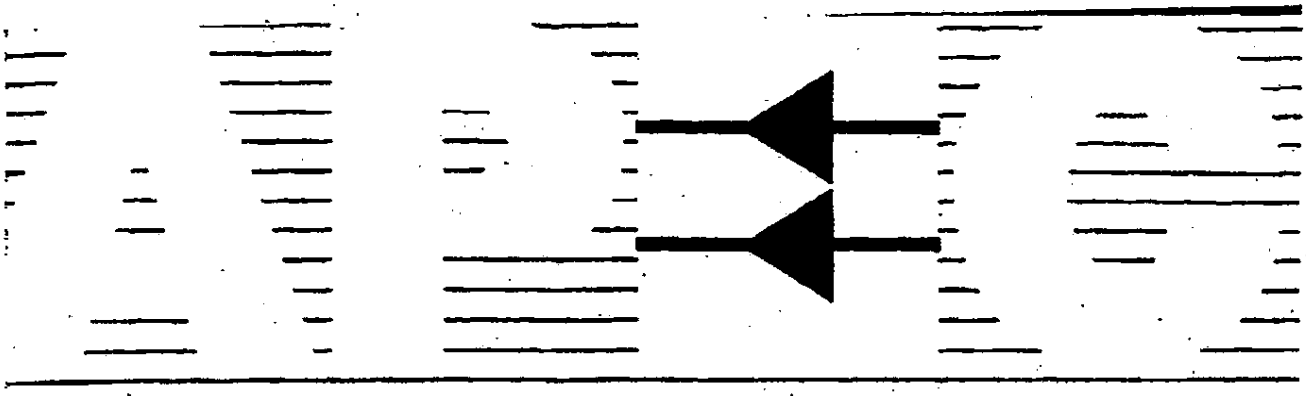

APEC '92

Seventh Annual Applied Power Electronics Conference and Exposition

Sponsored by the
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Electronics Society, the
IEEE Industry Applications
Society and the
Power Sources Manufacturers Association

Conference
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FOREWORD

On behalf of the APEC '92 Conference Committee, I would like to welcome you to the Seventh Annual Applied Power Electronics Conference and Exposition. We are proud to present this conference which has been specifically tailored to address the needs of the practicing power electronics professional.

This is the second year that APEC is co-sponsored by the IEEE Power Electronics Society, the IEEE Industry Applications Society, and the Power Sources Manufacturers Association. The broad and complementary interests of these three sponsors combine to create a unique forum for addressing all major aspects of *applied* power electronics incorporating product design, manufacturing, and marketing. This breadth is reinforced by the wide range of product applications discussed during the course of the conference extending from minature dc-to-dc power supplies to multi-Megawatt industrial motor drives.

This year's APEC qualifies as the "biggest ever" in several regards. More technical papers—a total of 114—are being presented at APEC '92 than ever before, selected by peer review from the nearly 200 submitted digests, another APEC record. This year's APEC is also more international than ever before with authors from 14 countries, and we extend a special welcome to all of our guests from outside the USA. The quality of the technical program is further enhanced by the inclusion of seven invited papers presented by well-known authorities in the field.

Another major aspect of the APEC technical program is the set of nine Professional Education Seminars offered on Sunday and Monday, presenting up-to-date information on topics spanning the breadth of APEC attendee interests. In addition, three rap sessions scheduled for Wednesday evening provide thought-provoking forums for participants to hear and be heard discussing important issues and trends affecting all of us in the power electronics profession.

The APEC '92 Exposition also merits special notice as the biggest ever, providing attendees a valuable opportunity to examine product offerings of more than 40 different power electronics manufacturers and service suppliers. In addition to the annual opening reception Monday evening, the Exhibition Hall plays host to lunches and afternoon refreshments on both Tuesday and Wednesday. Wednesday afternoon also brings the ever-popular Micro-Mouse contest in addition to informative product application seminars offered by several of the exhibitors.

The climax of the APEC '92 social calendar will occur Tuesday evening at Boston's excellent Museum of Science. The evening's events will include an Italian buffet dinner, a special showing of the Museum's Lightning! show, and ample opportunity to enjoy your colleagues' company while strolling among the Museum's many intriguing exhibits. For those interested in exploring Boston's rich historic and cultural heritage, the Westin Hotel is centrally located in downtown Copley Place to provide ready access to many of the most popular sights.

Finally, I would like to personally thank all of the members of the APEC Committee who have volunteered so much of their time and effort to organize every aspect of this conference. In addition, I wish to thank the staff of Courtesy Associates who have worked closely with our Committee to make this year's APEC the best ever, and we hope we have succeeded. That being said, APEC is still a young conference and we are anxious to receive new ideas from APEC attendees for future improvements. Even better, I invite you to consider volunteering to join our APEC '93 Committee to turn your ideas into action.

So . . . Welcome to APEC '92! May your week with us here in Boston be as enjoyable and personally rewarding as possible.

T.M. Jahns
General Chair

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†Manuscript unavailable for publication.

Off-line Power Integrated Circuit for International Rated 60-watt Power Supplies

Richard A. Keller
Power Integrations, Inc.
Mountain View, CA 94043

ABSTRACT - The first integrated circuit to economically combine a 700 volt, 3 Ω, high-speed power MOSFET switch with a full-function current programmed pulse width modulation control circuit is introduced. 60 watt 220 VAC input and 30 watt universal input flyback power supply designs are described.

I. INTRODUCTION

The power supply industry continues to push for higher power densities and the power components industry is responding in many ways. Passive components are adapting to the requirements of higher frequency and higher efficiency designs. Active component manufacturers are responding by producing parts with higher levels of integration to support these designs. For example, the PWR-SMP260 combines an 700 V, 3 Ω MOSFET, a fully featured current-mode controller, and an extended set of circuit and load protection features.

Digital synthesis is used in the protection features to eliminate many analog problems encountered in long time delays. This design has eliminated the need for large value, low leakage timing capacitors required for "latched" fault logic and "full cycle" soft start functions in other designs [1]. The integration of the logic-level MOSFET with the current-mode controller has allowed optimization of the gate drive design. It also allows the entire delay time from current-mode comparator to MOSFET output to be guaranteed without performance assumptions of an external gate driver.

Minimum external parts count is a goal for all high-density designs. The PWR-SMP260 requires seven external components including the off-line and bootstrap bias supplies. The integrated circuit is designed to connect directly to an optical coupler without any primary-side support circuitry.

Wide range bootstrap and off-line bias supplies make the integrated circuit ideal for universal input battery charging applications as well as power supply applications. The feature set required for battery charging applications contains all of the power supply requirements plus additional requirements. Battery chargers require a wide range output voltage, precise control of the output power, and a method of turning the charger on and off.

II. FUNCTIONAL DESCRIPTION

The integrated circuit combines a 700 V, 3 Ω MOSFET with a high speed current mode control circuit, high voltage off-line and bootstrap linear regulators, and power supply fault detection and recovery sequencing circuits. The block diagram is partitioned into two sections. The current mode control circuit and power MOSFET is shown in Figure 1 and the high voltage linear regulators and power supply fault detection and recovery sequencing circuits are shown in Figure 2.

A. The Power MOSFET

The gate drive requirements are significantly reduced because of the logic-level threshold voltage and very low Miller capacitance of the lateral geometry MOSFET. However, in an integrated solution the advantage of these characteristics is apparent to the user only as low bias supply current. The power supply designer need only be concerned with the output terminal characteristics of the MOSFET.

The conduction losses of the output MOSFET can be calculated from the on-state resistance ($R_{DS(ON)}$). $R_{DS(ON)}$ is 3 Ω for currents up to 1 A, and increases to 4 Ω at greater than 2 A. The practical limit for peak drain current in continuous operation is greater than 2 A. Switching losses due to the stored charge on the drain can be calculated from the 4.5 μJ of stored energy at 400 V. The stored charge in the output rectifier and transformer capacitance must be taken into account to get a good estimate of the total switching loss.

B. The Current Mode Controller

Many of the discrete components required in a current-mode controller design have been integrated in the summing junction function. The number of support components required for a production design has been reduced by at least a factor of two as compared to a "3842/3823 style" circuit.

1) *Summing Junction:* The output of the summing junction is a current source. The constant current flowing through R_C creates a fixed offset voltage. The current mode controller compares this offset voltage to the voltage across the primary current sense resistor R_S. The full scale summing junction output current (480 μA) times the ratio of the gain setting resistor R_C to the current sense resistor R_S will set the maximum current for the current mode controller and output MOSFET. If the

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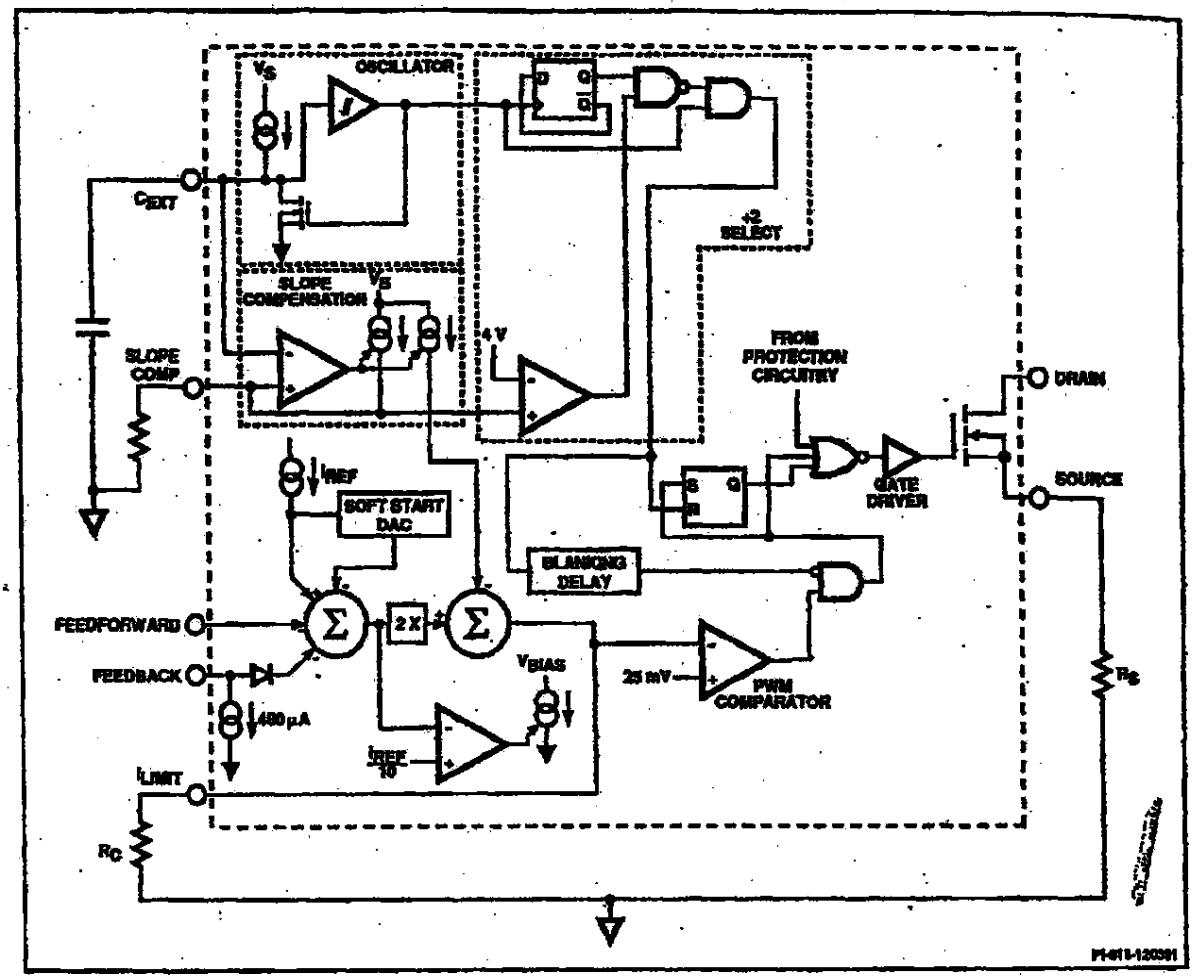

Figure 1. Detailed block diagram of the control and power output sections of the PWR-SMP260.

current sense resistor is 0.25 Ω and the maximum desired switch current is 2 A, then the gain setting resistor R_c should be

$$0.25\Omega \times \left(\frac{2A}{0.48mA}\right) = 1k\Omega. \quad (1)$$

The output of the summing junction can be controlled by injecting a current into the feed forward pin or the optical coupler pin. Current flowing into these pins will linearly decrease the current flowing from the summing junction output and correspondingly the peak current in the output switch. The optical coupler input pin has a current source associated with it. The current source insures that the optical coupler will be biased at 0.48 mA before the summing junction output current will be affected [2]. The voltage on these pins are 1.25 and 2 V respectively and have input impedances of less than 1 kΩ. The feedforward and optical coupler currents have a gain of 2 within the summing junction.

The part is designed for a secondary-referenced error amplifier with optical feedback. However, primary side regulation can be achieved by adding a primary-referenced error amplifier circuit. A simple error amplifier can be implemented by connecting a Zener diode between the bootstrap bias supply and the optical coupler pin. The current source on the pin will bias the Zener diode and the diode will control the bootstrap bias voltage that is proportional to the output voltage via the transformer turns ratio.

The feedforward pin can be used for control loop compensation for changes in input voltage. A separate pin is provided so that open loop compensation is available when the secondary regulator control loop is open. A constant input power regulator for wide ranges in input and output voltage can be constructed using this feature. This feature along with a wide bootstrap bias supply range is very useful in battery charging applications.

The summing junction also has internal control inputs from the soft start digital to analog converter and the slope compen-

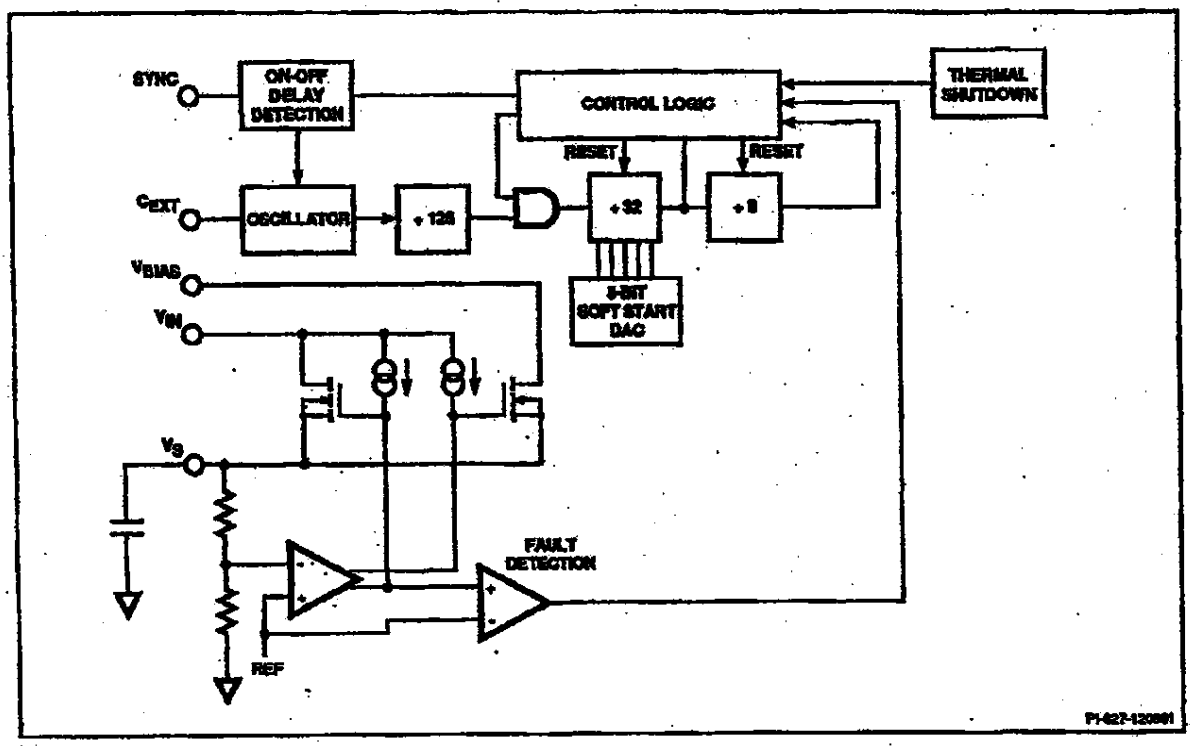

Figure 2. Detailed block diagram of the internal regulator and protection circuitry of the PWR-SMP260.

sation circuit. The soft start digital to analog converter will inject 100% of the reference current into the summing junction at the beginning of the soft start sequence and incrementally decrease the soft start injection to zero.

The slope compensation causes the sum junction output current to be linearly decreased over the programmed pulse width (Figure 3). The rate of decrease is programmable with the slope compensation resistor value. The shape of the compensation current is the same as the oscillator waveform. Slope compensation is inhibited and 50% maximum duty cycle is selected when the slope compensation pin is connected to V_S.

2) *Comparator and Blanking Time:* The key elements of the current-mode control circuit are the comparator, R-S flip flop, gate driver, and output transistor. The two parameters of interest [3] are the delay time from the comparator input to the MOSFET output and the leading edge blanking time. The delay time of current sense comparator, gate driver and output MOSFET are all specified together in an integrated controller. A discrete design must consider the tolerance of each part, also the effect of the printed circuit board layout capacitance and inductance on circuit delay time. Other advantages of an integrated solution are the gate driver is optimized for the output transistor characteristics. An integrated design also removes the chance of noise injection in the critical gate drive printed circuit board layout.

Leading edge blanking allows the turn on current transient to stabilize before the output of the current mode comparator is connected to the R-S flip flop. The start of the blanking time is the turn on of the MOSFET. The blanking time is specified as the maximum time the comparator input can exceed the comparator threshold and recover to 100 mV below the threshold and not have the output MOSFET switch off. The blanking time is designed to allow the turn on current spike to recover in a flyback power supply operating in continuous conduction mode with an "ultra fast" rectifier. A current spike waveform similar to Figure 4 will not cause a circuit malfunction.

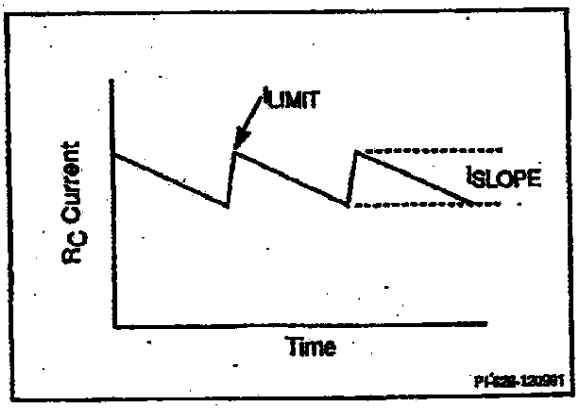

Figure 3. Slope compensation current relationships.

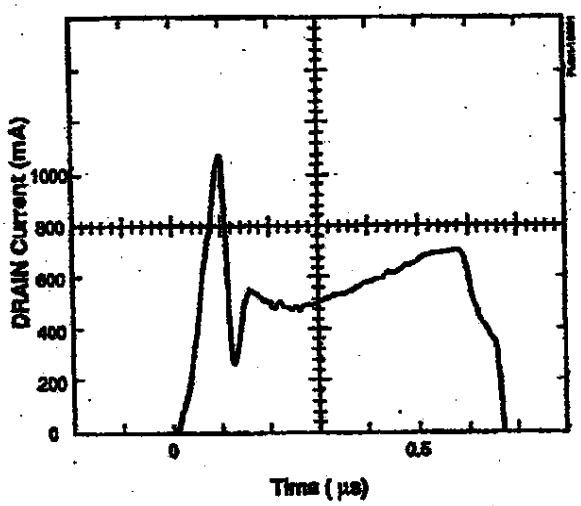

Figure 4. Leading edge current spike example.

3) *Maximum Duty Cycle:* The maximum duty cycle is user programmable. If a 50% maximum duty cycle is desired connect the slope compensation pin to the V_s internal bias supply voltage. A frequency divider flip-flop will be inserted between the oscillator and the current mode R-S flip-flop the maximum duty cycle will be 50%. The oscillator timing capacitor will need adjustment so that the oscillator will run at twice the output frequency.

If a 90% maximum duty cycle is desired connect a resistor between the slope compensation pin and common. The resistor determines the amount of slope compensation current flowing in the output of the summing junction. The slope compensation has the effect of reducing the current flowing from the summing junction linearly with time. Equation (2) shows how to calculate the desired slope compensation resistor value.

$$R_{SLOPE} = \frac{1.75V}{I_{SLOPE}} \qquad (2)$$

A current mode control loop operating in the continuous conduction mode with duty cycles over 50% requires slope compensation for stability [4]. The amount of slope compensation is a function of the slope of the magnetizing current flowing in the MOSFET. Circuits that have discontinuous conduction over the entire duty cycle range do not need slope compensation. However, in noisy environments, a small bypass capacitor is recommended.

4) *Minimum Load:* Current mode control has a well known problem of regulating at minimum load due to minimum pulse width. A minimum width pulse will transfer a incremental amount of power to the output every time the power switch is turned on. Operating at no load usually require compromises that usually take shape as a pre-load resistor on the output or the switching frequency being reduced by initiating a subharmonic oscillation. The pre-load solution is unacceptable in modern thermally limited high efficiency designs. The subharmonic oscillation, often called "hiccup mode" is equally unacceptable because of possible audible noise emissions.

The PWR-SMP260 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added (Figure 1). A shunt regulator is activated when the summing junction current falls below 12% of full scale. The shunt regulator will increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale. Figure 5 shows the load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The control loop gain path is shown in Figure 6. The gain of the minimum load regulator has been matched to the gain of the current mode switching regulator. This allows the control loop dynamics remain the same whether the minimum load circuit is active or not active.

The output transient load response is shown in Figure 7. Note that at light load the gain of the switch mode path decreases but the gain of the minimum load path remains the same and the transient load response is not significantly degraded. A interesting side effect of the minimum load circuit is its effect on bias supply power during a transient. The power consumed from the bias supply is greater than the average of the two states when the period of the transient is close to the control loop response time.

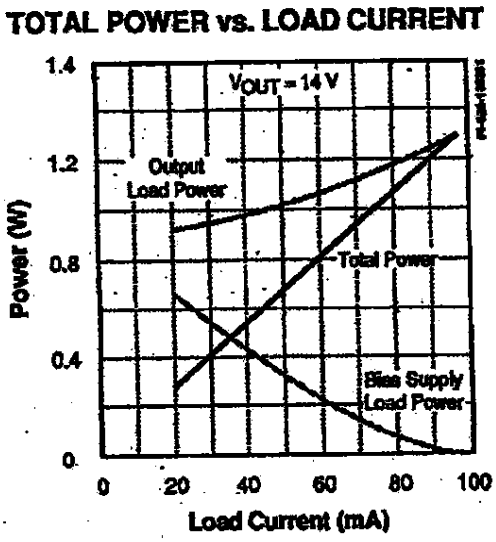

Figure 5. Minimum load transfer effect.

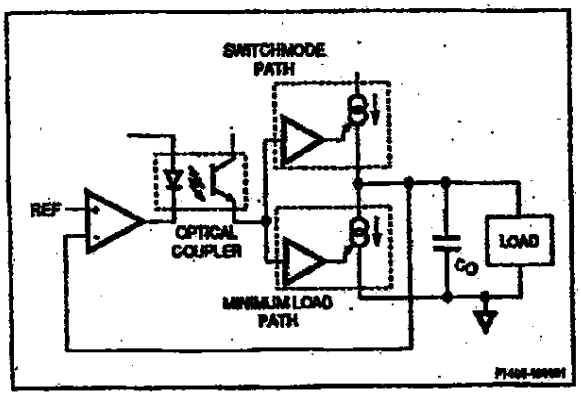

Figure 6. Current mode and minimum load control loop.

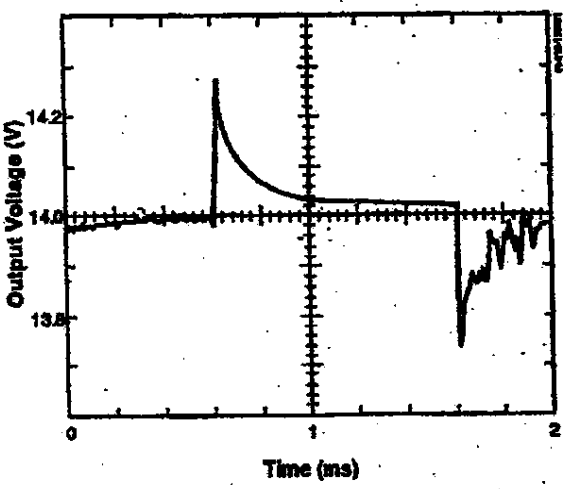

Figure 7. Minimum load output transient response.

The control loop overshoot, settling time and transient repetition rate affect this characteristic. The bias supply load power vs load transient frequency for a 50% duty cycle is shown in Figure 8. The best load transient response occurs when the capacitance on the bias supply is a minimum.

C. Oscillator

The oscillator-switching regulator circuit is designed for optimum performance between 30 and 400 kHz. The oscillator waveform is a sawtooth with a slow rise from zero to 1.75 V followed by a rapid discharge. The oscillator will operate at twice the power supply frequency when the 50% maximum duty cycle option is selected. The oscillator frequency is set with a timing capacitor. The oscillator timing capacitor value can be estimated by dividing 94 µF-Hz by the desired clock frequency.

The oscillator can be synchronized to a clock that is running at a higher frequency. A short pulse of less than 1 µs is applied to the SYNC pin to terminate the clock cycle. The SYNC pin has a CMOS logic level and is negative edge sensitive. However, if the signal is held low for longer than 10 µs, it will be interpreted as an on-off signal sending the circuit into a power down state which continues for as long as the signal is low. The interface circuits for isolated synchronization and ON/OFF signals are shown in Figure 9.

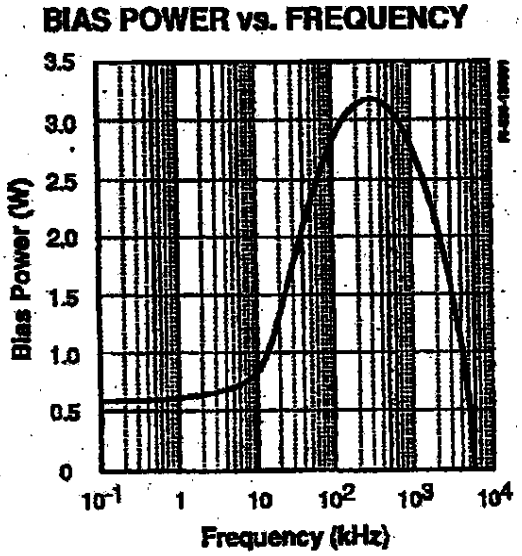

Figure 8. Effect of load transient frequency on bias power.

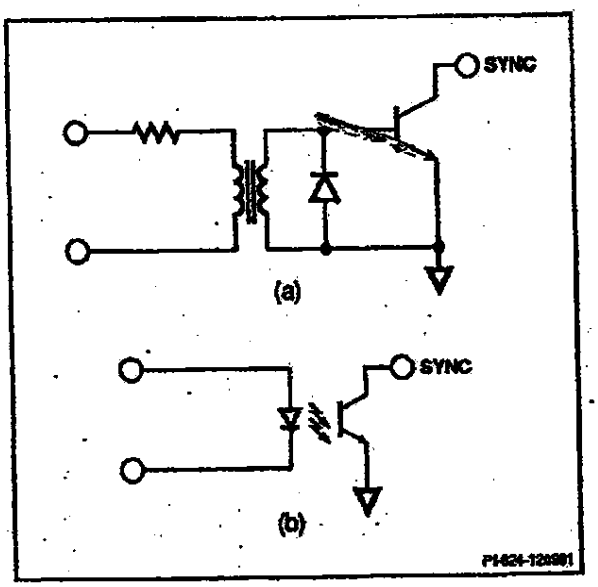

Figure 9. (a) Synchronization and (b) ON/OFF interface circuits.

D. Bias Regulators/Protection Circuitry

The high voltage linear regulators and power supply fault detection and recovery sequencing circuits are shown in the block diagram Figure 2.

1) *Bias Regulators:* The linear regulator for the internal supply voltage V_s has two sources of power. They are the bootstrap bias supply and the off-line high voltage supply. The regulator has a built-in preference for the bootstrap bias supply. Should the bias supply be incapable of supplying the total requirement, the remaining current will be sourced from the off-line voltage. A small current source connected to the V_{IN} pin is the only current consumed from the off-line voltage when the off-line regulator is turned off.

The internal V_s supply voltage will be operational. This occurs at a minimum V_{IN} voltage of 36 V. This is independent of the bootstrap bias supply voltage.

Reverse current through the bootstrap bias regulator transistor has been eliminated. The V_s supply will not be loaded by circuitry powered from the bias supply at turn-on. Additional primary-referenced circuitry may be powered from the bootstrap bias supply without affecting the operation of the control circuit. If reverse current flow were not blocked the V_s could be loaded down and prevent the undervoltage lockout signal from releasing the switch mode regulator.

2) *Protection Functions:* Protection features include input under voltage lockout, over temperature fault, output under voltage fault and output over current protection consistent with cycle by cycle peak limiting of the switch current. The input under voltage lockout holds the gate of the output MOSFET low and resets the soft start counter chain until the V_s supply voltage is within its valid operating range. The fault conditions control the functioning of the "latched fault logic" and restart delay sequence.

The over temperature protection circuit monitors the junction temperature of the power MOSFET and signals a fault when the preset temperature is exceeded. The fault will continue until the junction temperature drops below a lower level. During the time a fault is sensed, the output switching MOSFET is turned off and the soft start counter chain is reset. The power consumption of the control circuit is reduced during a fault to limit self heating of the off-line regulator.

A fault condition also will be declared when the bootstrap bias voltage drops low enough to draw current from the off-line regulator. This condition indicates that the output voltage is significantly out of regulation and an overload condition exists. The fault condition is not declared when the bootstrap bias voltage is low and the minimum load circuit is active. The bootstrap bias voltage can be momentarily be pulled low during a minimum load transient which would erroneously indicate a fault.

The "latched fault logic" turns off the output MOSFET, reduces the power consumption of the control circuit and starts the restart delay sequence. When the counter reaches 28,672 power supply equivalent cycles the soft start sequence starts.

The power up sequence is between 3969 and 4096 power supply equivalent cycles long. During this time the switching regulator circuits are enabled and the bootstrap bias supply should reach its valid operating range. The bootstrap bias voltage is monitored at the end of this period. If the voltage is below the regulation voltage, a fault is signaled and the cycle repeats. This characteristic produces a foldback current limit function as shown in Figure 10. This function is very effective for limiting the dissipation in over load and short circuit conditions.

3) *Soft Start:* During power up the circuit has an optional soft start function. Soft start is enabled by connecting the soft start pin to the V_s pin and disabled by connecting it to common. When soft start is disabled, the maximum switch current is available for power transfer to the output. When the output voltage is low this usually puts the transformer deep into continuous conduction mode. The circulating current rises rapidly and the transformer core can be driven into saturation. The output rectifier also experiences a large current and thermal transient.

When soft start is enabled the maximum output switch current is programmed linearly increasing from zero to maximum in 4096 power supply equivalent clock cycles. A 5 bit digital-to-analog converter controls the current available from the summing junction during the power up period.

Power up is the time when most power supplies fail. The soft start function reduces all of the power supply component peak stresses during the power up sequence. This should produce a power supply with a superior demonstrated reliability.

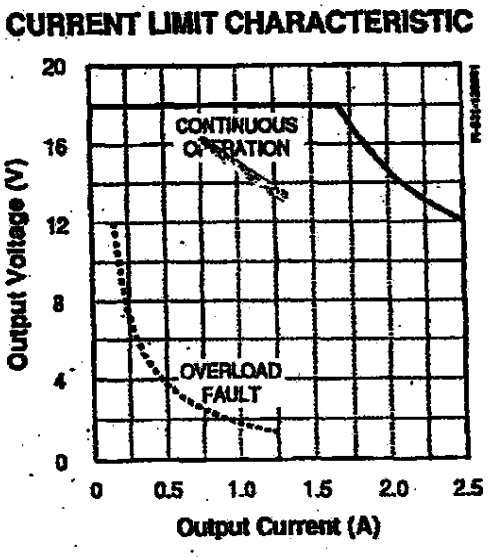

Figure 10. Foldback current limit for flyback operation.

III. CONTROL LOOP MODEL

The current mode control loop can be modeled as a controlled current source driving the total output capacitance of the power supply as shown in Figure 6. The transfer function will have a one pole response and have 90 degrees of phase margin [5].

The gain of the optical coupler is equal to the current transfer ratio (CTR). The CTR for a 4N26 optical coupler is typically 0.5 with a range of 0.3 to 1 when operating at output currents between 0.5 to 0.75 mA[6]. The input impedance of the optical coupler port on the integrated circuit is kept low so that the pole formed by the optical coupler capacitance will be as high frequency as possible.

Equation (3) describes the output voltage to LED current gain of the typical TL431 error amplifier circuits shown in Figures 11 and 12.

$$\frac{I_{LED}}{V_O} = \frac{1 + \left[\left(\frac{1}{2\pi \times R_5 \times C_1}\right) \times \left(1 + \frac{f}{\left(\frac{1}{2\pi \times R_2 \times C_1}\right)}\right)\right]}{\frac{f}{R_1}} \quad (3)$$

The error amplifier has two forward gain paths. The first is through the amplifier section, which is dominant until the amplifier reaches unity gain. The second is directly from the output to the optical coupler. At frequencies greater than the unity gain frequency the signal path directly from the output to the optical coupler dominates.

Circuits that have an output π filter should partition the error amplifier. The optical coupler should be connected to the input of the π filter and the voltage seasing divider can be connected to the output of the π filter. This insures that the two poles of the output π filter will not be present in the high frequency response of the error amplifier [7].

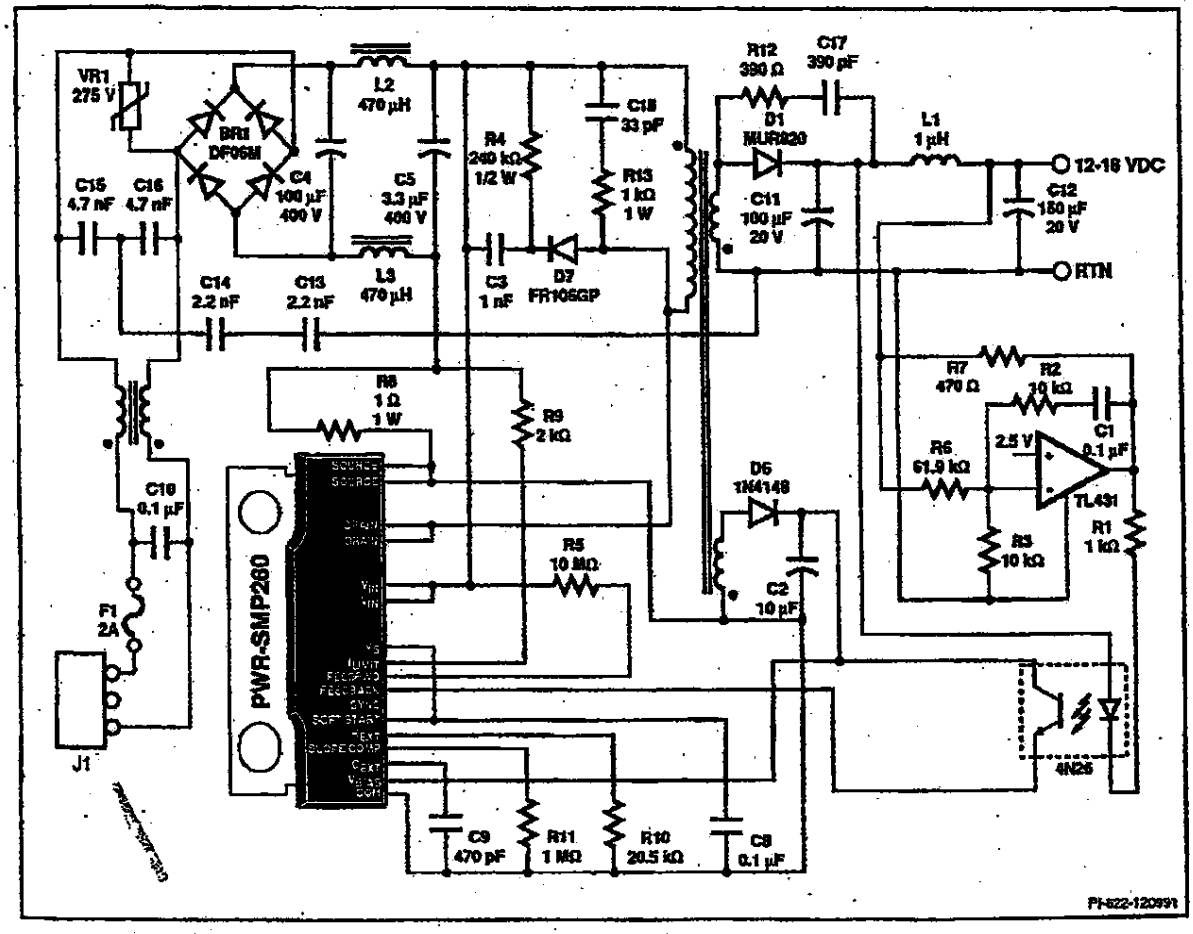

Figure 11. Flyback converter circuit using the PWR-SMP260.

IV. PACKAGE AND LAYOUT CONSIDERATIONS

The integrated circuit package is a single in-line power tab package 30 mm wide by 3.5 mm thick by 20.2 mm high. The high-voltage pins have a 3.1 mm gap between them for international safety spacing requirements. The pins are on 1.27 mm centers with a 2.54 mm stagger bend. This allows a printed circuit board to be designed with a high voltage pad to pad spacing greater than the required 2.5 mm for IEC950. A pad diameter of 1.52 mm and a hole size of 1.02 mm can be used.

The power tab is electrically connected to the source of the output MOSFET. An insulator between the heat sink and the power tab is not required. Connecting the heat sink to the circuit common is also advantageous for EMI suppression.

V. FEATURES APPLIED TO POWER SUPPLY AND BATTERY CHARGING APPLICATIONS

The wide range in bootstrap bias supply voltage 8 to 30 V relieves the granularity of the output to bias winding turns ratio. Battery charging applications require a wide range output voltage to track the terminal voltage of a charging battery.

The bootstrap bias supply under voltage shutdown can prevent a discharged battery with a shorted cell from being charged. The shorted cell will drop the battery terminal voltage below the minimum output voltage and this function will prevent over heating and possible rupture of the remaining cells.

The electronic on/off is also useful in system applications such as battery chargers controlled by microcontrollers. The synchronizing and on/off control pin can be driven using a transformer or optical coupler as shown in Figure 9.

The 90% duty cycle option allows applications to operate down to lower input voltages with some compromise in output ripple voltage and rectifier stress. Built-in slope compensation reduces the external circuitry required to implement this function.

Minimum load control prevents leading edge blanking from requiring a minimum output power. Feedforward control allows for open loop compensation for variations in the input voltage. A design with the correct transformer inductance and operating frequency will provide an open loop constant power transfer circuit. The shutdown automatic restart function requires that the bootstrap bias supply be above 8 V within 4096 equivalent clock cycles. This puts a limit on the amount of capacitance that can be charged during this time.

VI. THE 60 WATT POWER SUPPLY

The schematic for the flyback power supply is shown in Figure 11. The Line and Load Regulation is <0.1%. The same circuit can be designed to operate continuously over the universal input voltage range of 85 to 265 VAC_{RMS} by changing the transformer turns ratio. However, the increase in input voltage range reduces the output power to 30 W. The line, load regulation is <0.1%. The 30 W circuit has been demonstrated within an enclosure with dimensions of 32.5 x 60 x 95 mm.

A forward converter can be constructed by replacing the secondary-side components of Figure 11 with those shown in Figure 12. The output inductor is common with the bias supply to insure minimum load operation.

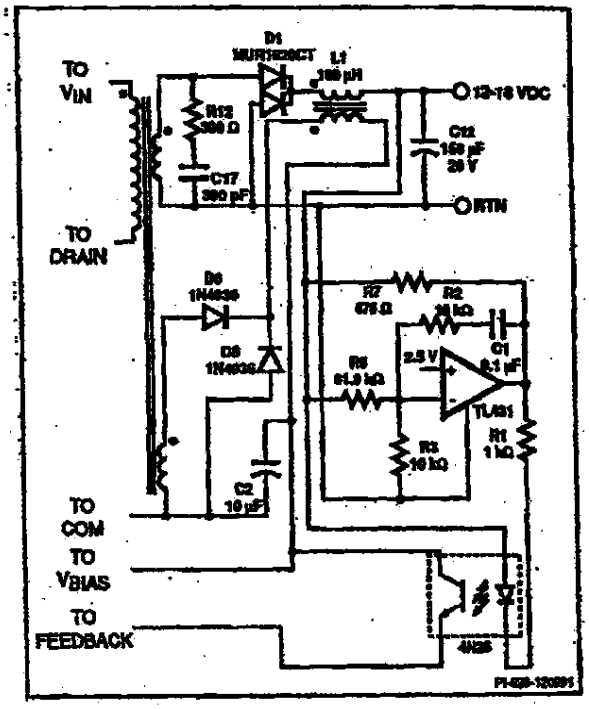

Figure 12. Modifications to the secondary-side circuitry to form a forward converter.

REFERENCES

[1] Bill Andreycak and Larry Wolford, "High frequency PWM controllers - a new enhanced generation," *HFPC Proceedings*, pp. 94-107, June 1991.

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[3] Bill Andreycak and Larry Wolford, "High frequency PWM controllers - a new enhanced generation," *HFPC Proceedings*, pp. 94-107, June 1991..

[4] S.P. Hsu, A. Brown, L. Rensink, and R.D. Middlebrook, "Modelling and analysis of switching DC-DC converters in constant-frequency current-programmed mode," *Proceedings of the IEEE Power Electronics Specialists Conference*, pp. 284-301, 1979.

[5] R. B. Ridley, "A new continuous-time model for current-mode control," *Power Conversion and Intelligent Motion Conference Proceedings*, pp. 455-464, October 1989.

[6] R.B. Ridley, "Secondary LC filter analysis and design techniques for current-mode-controlled converters," *IEEE Transaction on Power Electronics*, Vol. PE-3, No. 4, pp. 499-507, October 1988

[7] ibid.

DX 70

PWR-SMP240

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 40 W from rectified 220/240 VAC input, 20 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller
- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-in Self-protection Circuits
- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

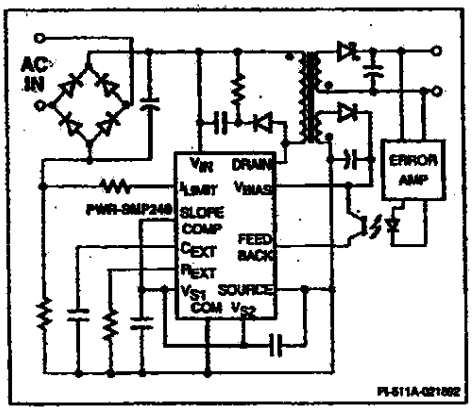

Figure 1. Typical Application

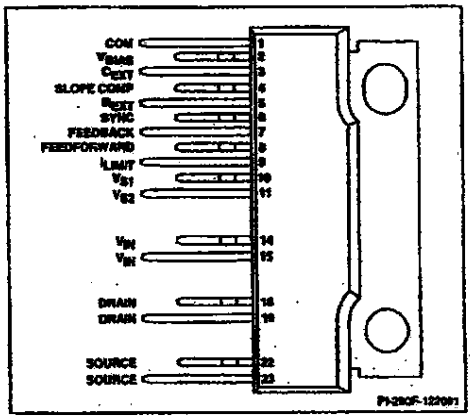

Figure 2. Pin Configuration

Description

The PWR-SMP240, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP240 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP240 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP240WTC	23-pin PWR SIP	0 to 70°C

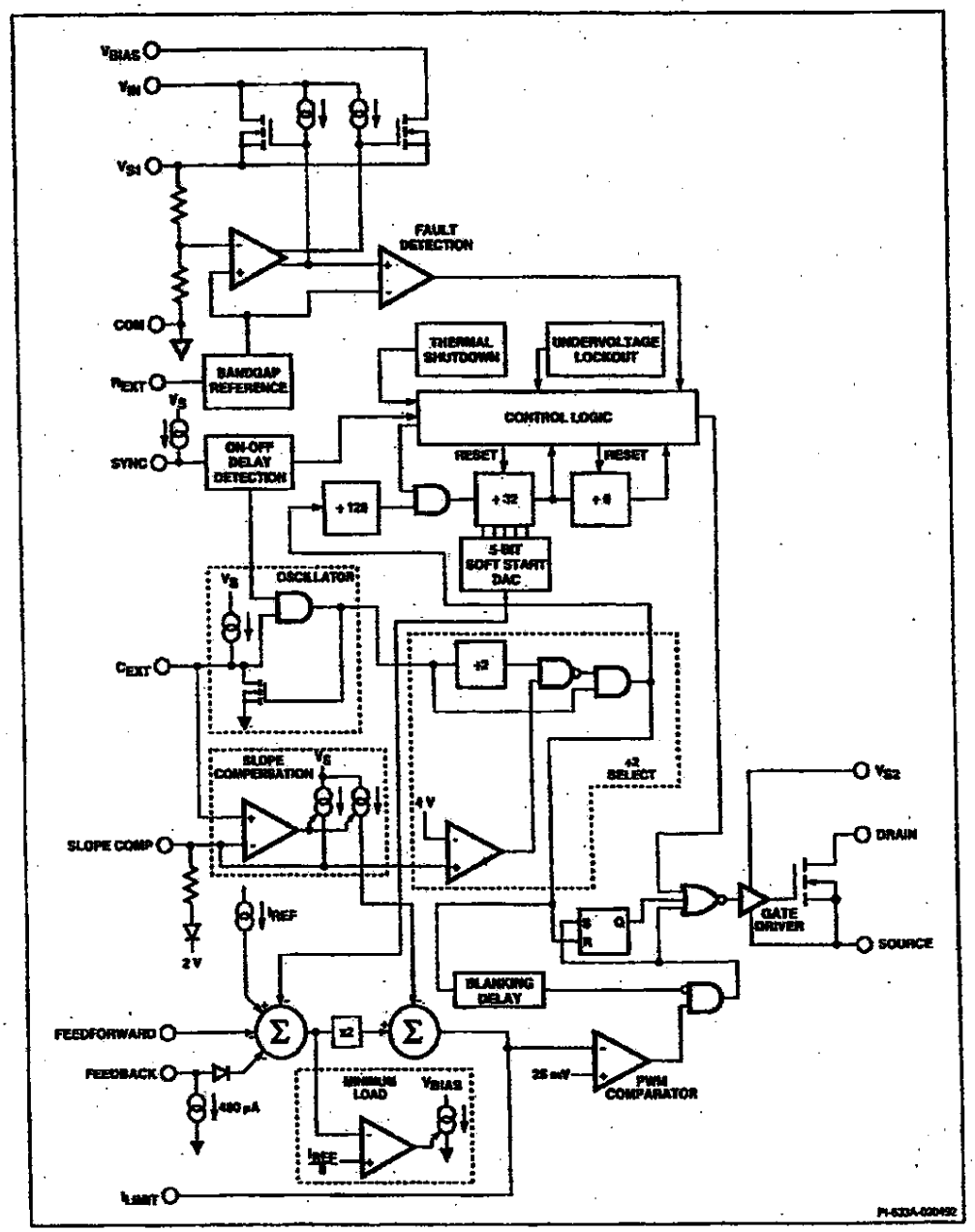

Figure 3. Functional Block Diagram of the PWR-SMP240.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
V_{BIAS} is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance between C_{EXT} and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connection through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between R_{EXT} and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
I_{LIMIT} is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
V_{S1} is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via V_{S2}. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open DRAIN of the output MOSFET.

Pin 22, 23:
The SOURCE is the high-current return for the output MOSFET.

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PWR-SMP240 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP240 Functional Description (cont.)

Oscillator
The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care should be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator
The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start
The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the limit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit
The undervoltage protection circuit insures that the output transistor is off until the V_{IN} is regulated.

Overtemperature Protection Circuit
The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

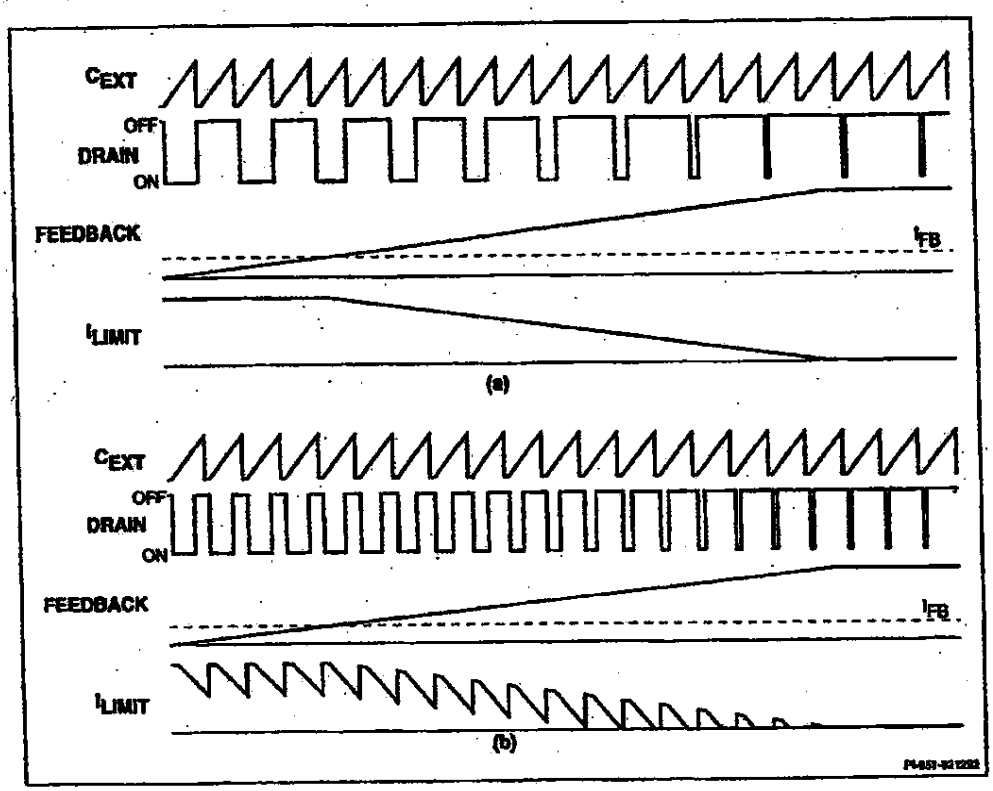

Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode, and (b) 90% Maximum Duty Cycle Mode.

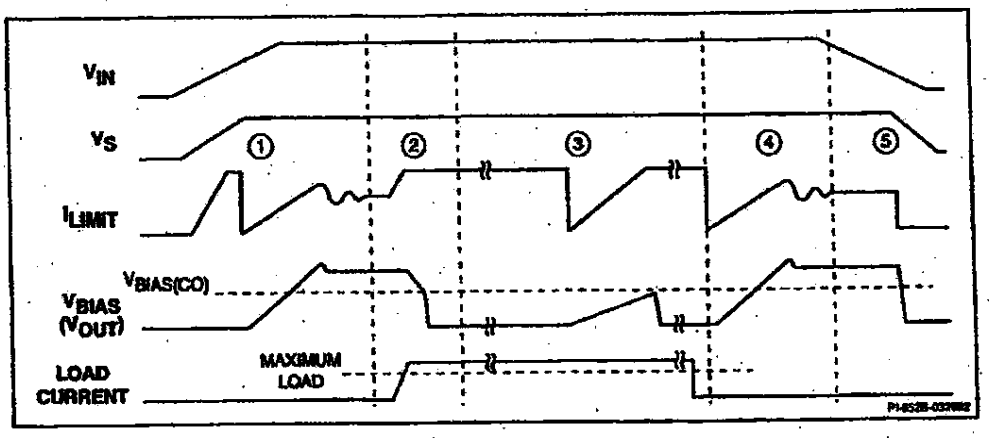

Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

20 W, Universal Off-line Power Supply

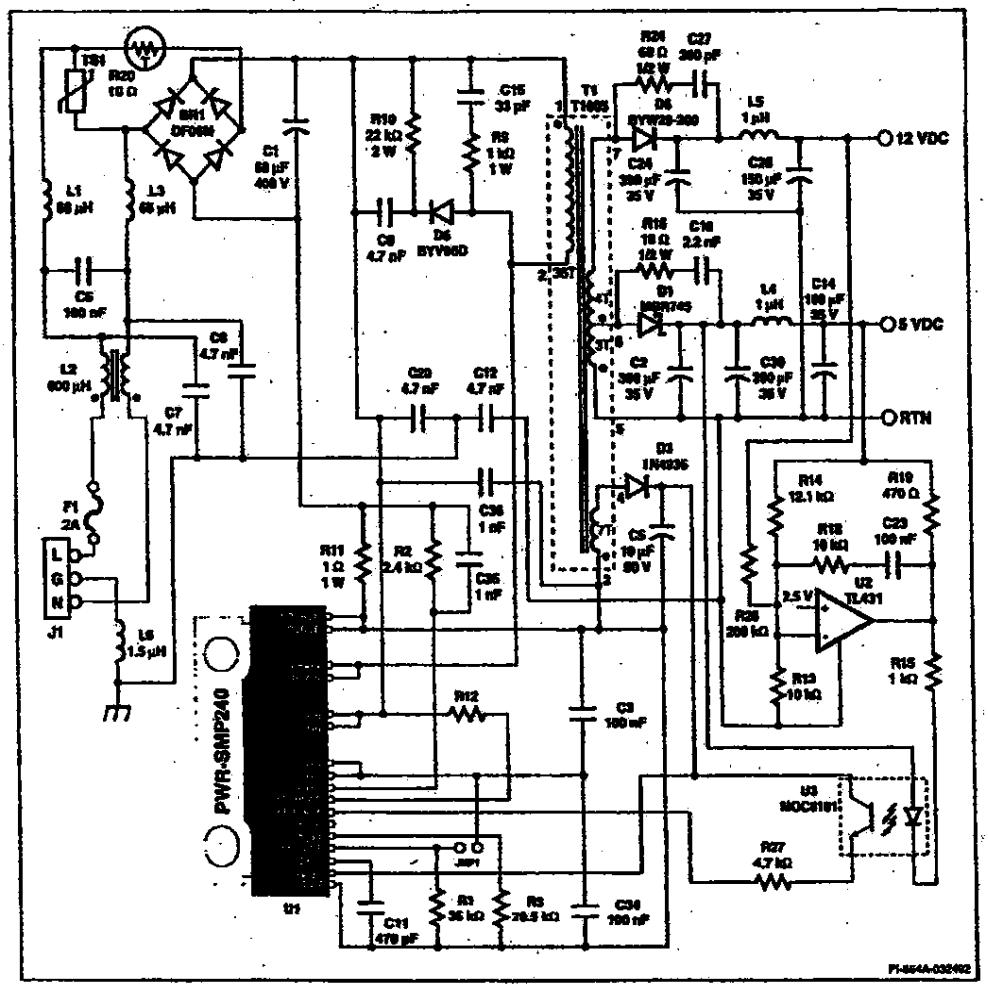

Figure 6. Schematic Diagram of a Single Output 20 W Supply Utilizing the PWR-SMP240.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 20 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SI}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SI}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{MAS} supply through the optocoupler U3.

The current-mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

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TOTAL POWER vs. LOAD CURRENT

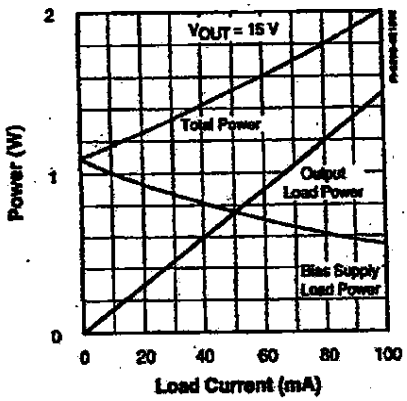


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP240 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{SI} when V_{JH} is between 12 and 20 VDC. The V_{SI} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{SI} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

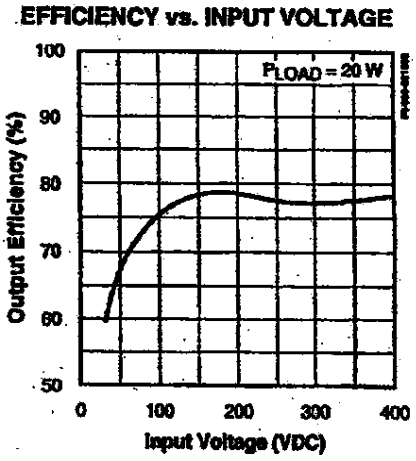
During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

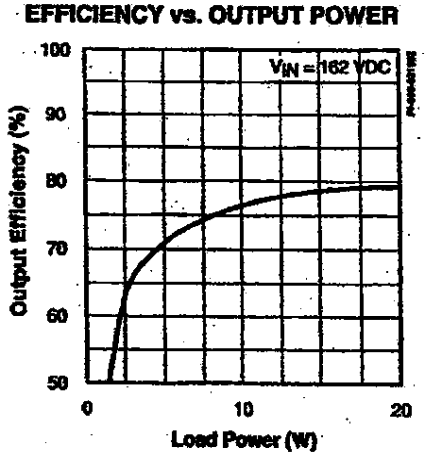
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL8 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP240. Complete supply specifications are included, as well as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)





ABSOLUTE MAXIMUM RATINGS

DRAIN Voltage ..... 700 V
V_{EX} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 2 A
Storage Temperature ..... -65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_{AB} = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(SJ)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{ILIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S, FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{ILIMIT}	V_{ILIMIT} = 150 mV		75		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
PULSE WIDTH MODULATOR (CONTINUED)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(ML)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity				±0.5		lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	TYP	MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C			5	Ω
			T_J = 115°C			8.5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		1.2	1.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			200		pF
Output Stored Energy	E_{OSS}				1500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

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NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP240 is connected to a high-voltage power source when the test circuit is activated.

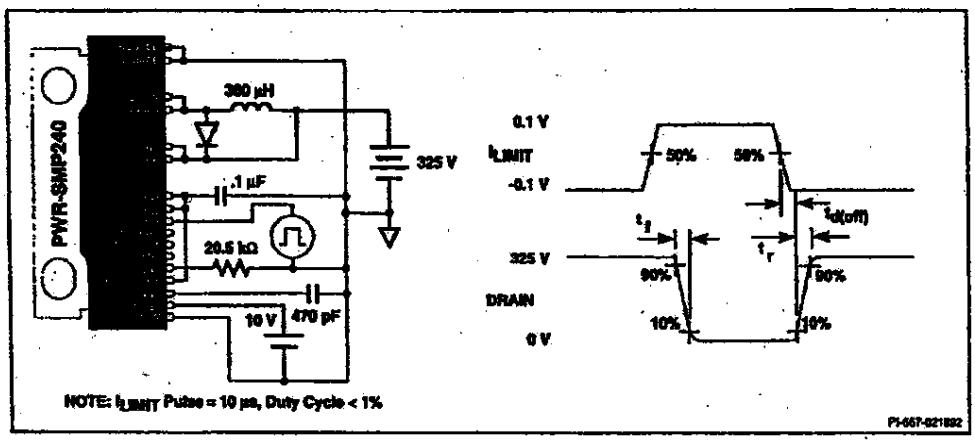
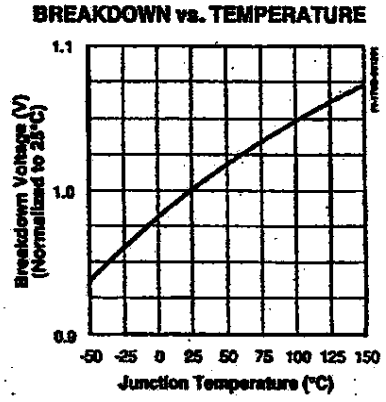
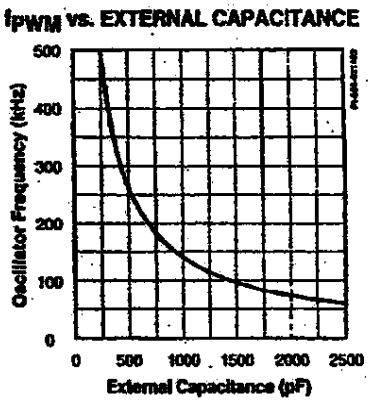
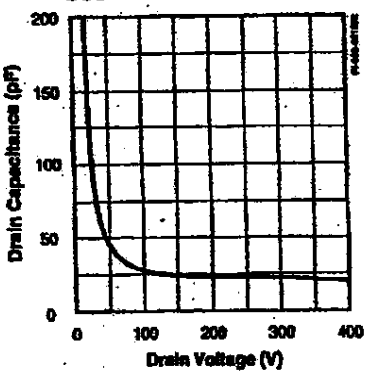


Figure 8. Switching Time Test Circuit.

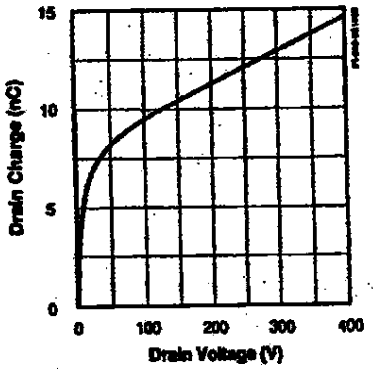




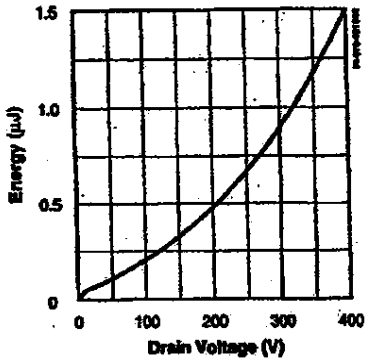
C_{OSS} vs. DRAIN VOLTAGE



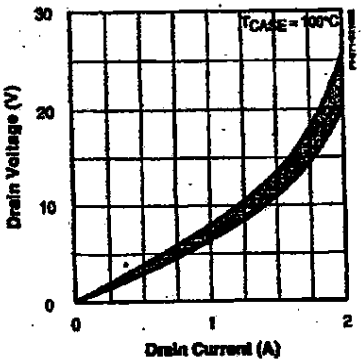
DRAIN CHARGE vs. DRAIN VOLTAGE



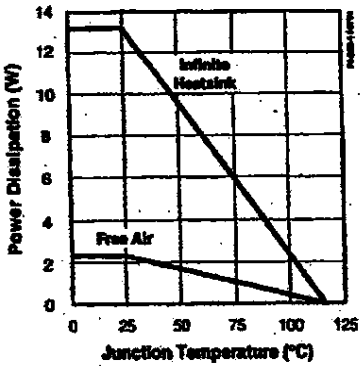
DRAIN CAPACITANCE ENERGY



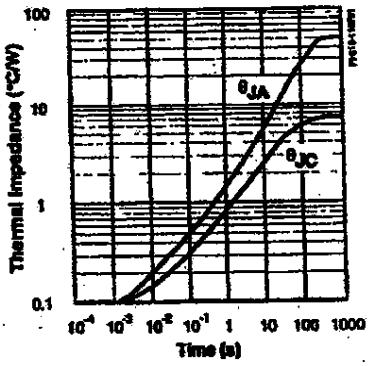
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



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FCS1685831

DX 74

PWR-SMP260

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 60 W from rectified 220/240 VAC input, 30 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller
- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-in Self-protection Circuits
- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

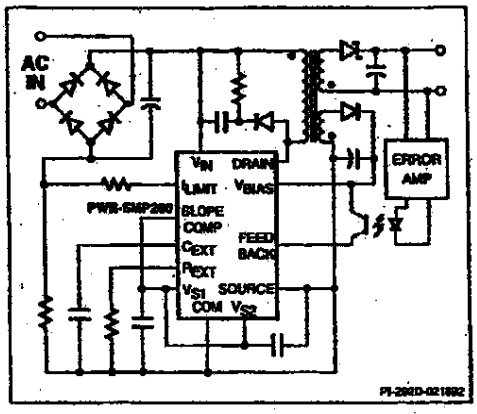

Figure 1. Typical Application

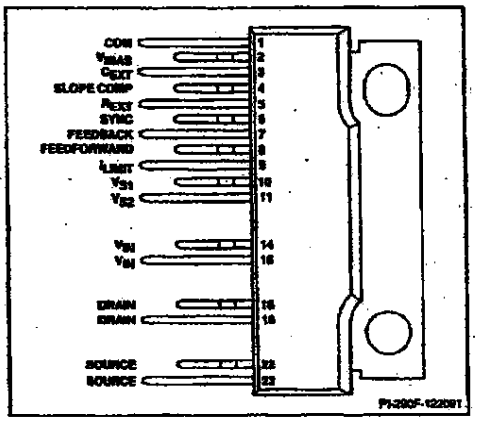

Figure 2. Pin Configuration

PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP260WTC	23-pin PWR SIP	0 to 70°C

Description

The PWR-SMP260, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP260 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP260 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

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Case No. 04-1371-JJF
DEFT Exhibit No. DX 74
Date Entered _____
Signature _____

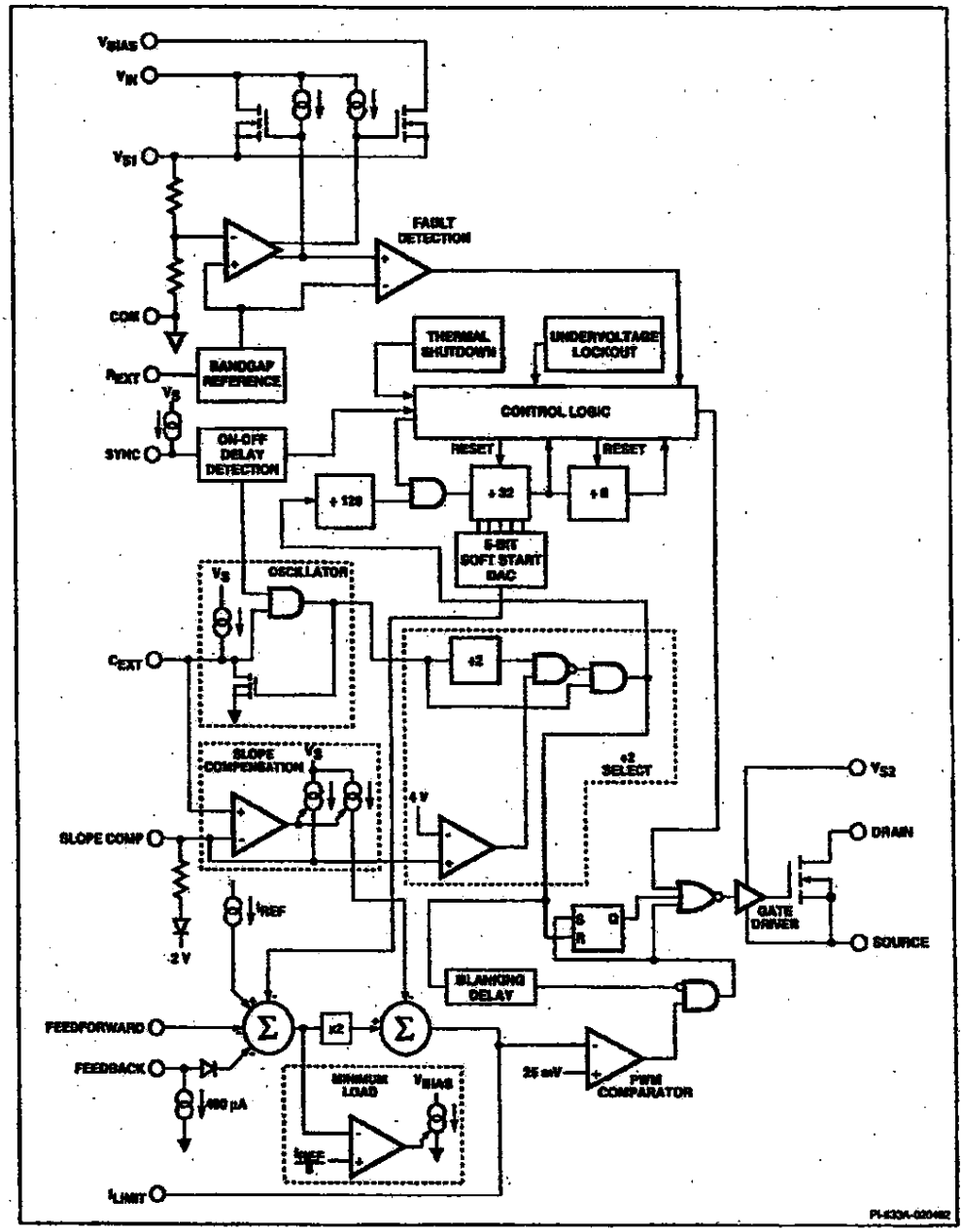

Figure 3. Functional Block Diagram of the PWR-SMP260.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
V_{BIAS} is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance between C_{EXT} and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connection through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between R_{EXT} and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
I_{LIMIT} is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
V_{S1} is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via V_{S2}. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open **DRAIN** of the output MOSFET.

Pin 22, 23:
The **SOURCE** is the high-current return for the output MOSFET.

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PWR-SMP260 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP260 Functional Description (cont.)

Oscillator
The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care should be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator
The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start
The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the limit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit
The undervoltage protection circuit insures that the output transistor is off until the V_{IN} voltage is regulated.

Overtemperature Protection Circuit
The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

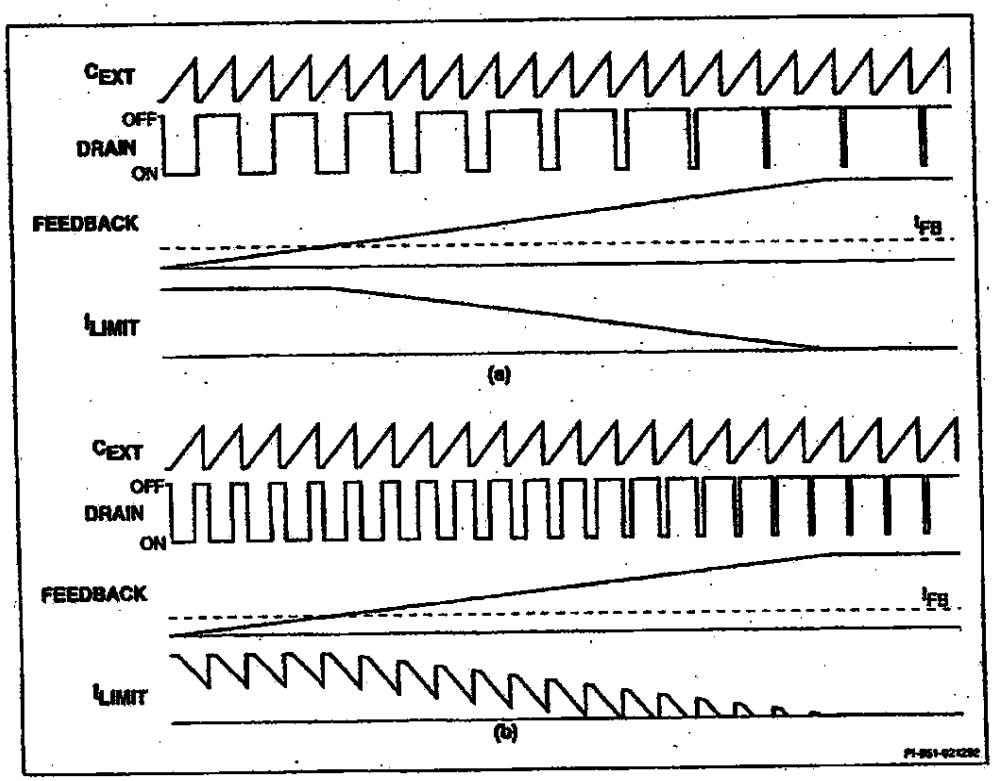

Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode. and (b) 90% Maximum Duty Cycle Mode.

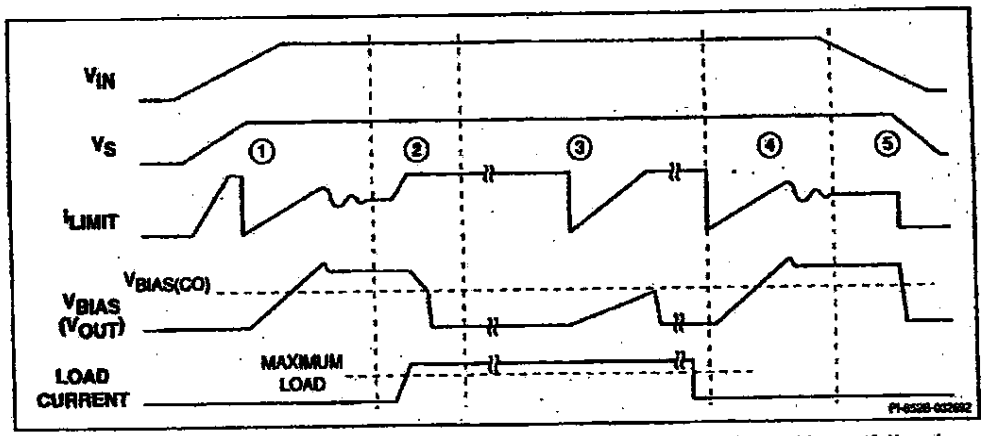

Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

30 W, Universal Off-line Power Supply

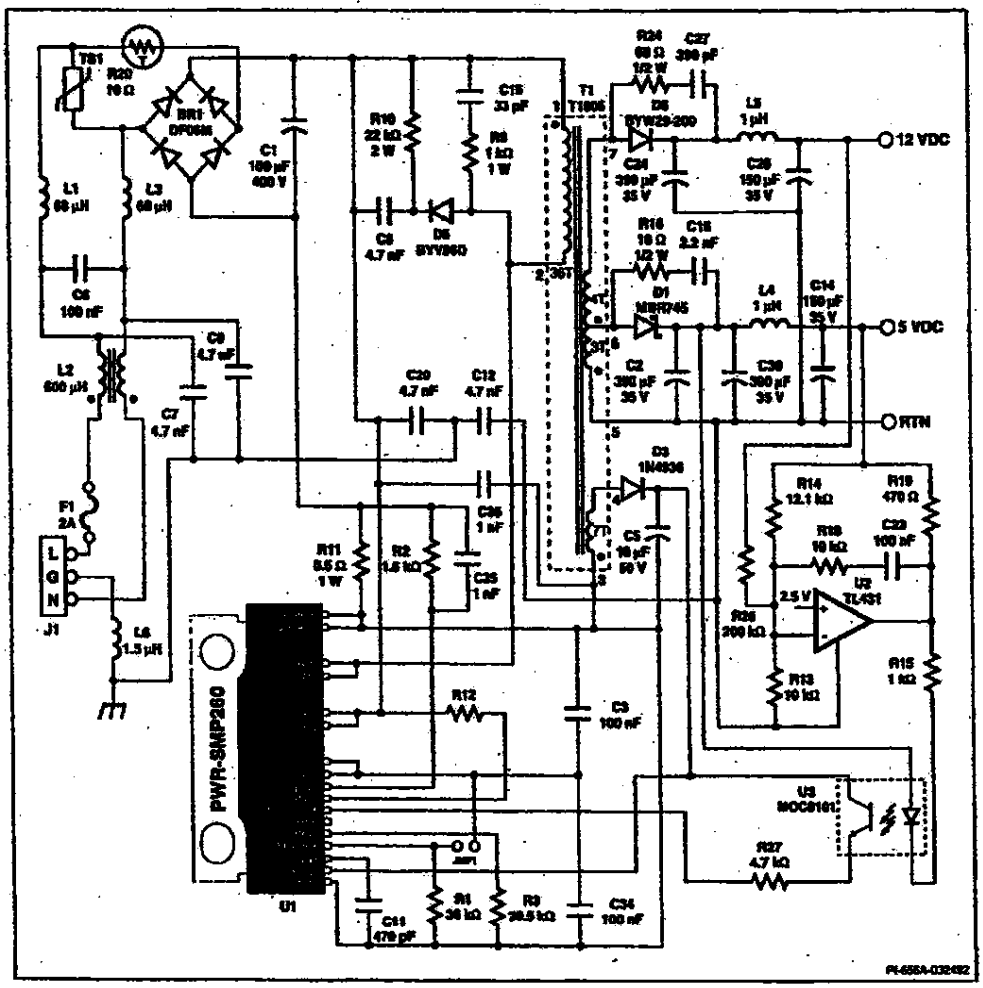

Figure 6. Schematic Diagram of a Single Output 30 W Supply Utilizing the PWR-SMP260.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 30 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SI}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SI}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{BIAS} supply through the optocoupler U3.

The current mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

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TOTAL POWER vs. LOAD CURRENT

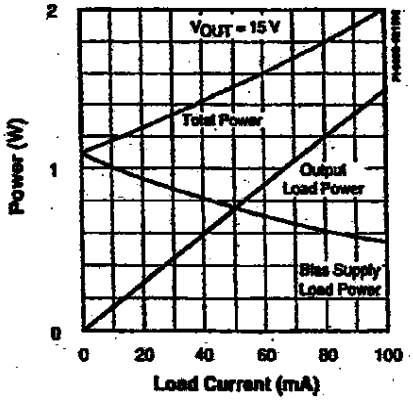


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP260 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{SS} when V_{BR} is between 12 and 20 VDC. The V_{SS} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{SS} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

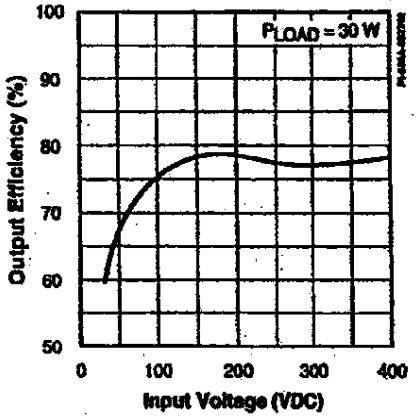
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

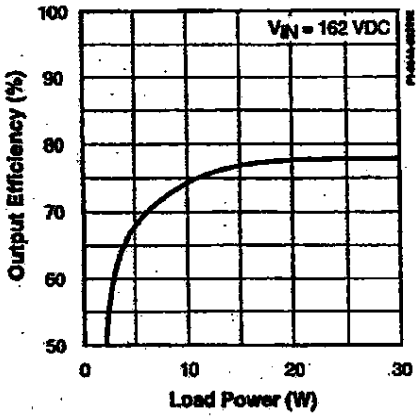
The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL7 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP260. Complete supply specifications are included, as well as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)

EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



ABSOLUTE MAXIMUM RATINGS

DRAIN Voltage ..... 700 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 3 A
Storage Temperature ..... -65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_A = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(S)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{LIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S, FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{LIMIT}	V_{LIMIT} = 150 mV		75		ns

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Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits			Units
			MIN	TYP	MAX	
PULSE WIDTH MODULATOR (PWM)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(MIN)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity				±0.5		lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

FCS1685815

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C			3	Ω
			T_j = 115°C			5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		2	2.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			280		pF
Output Stored Energy	E_{OSS}				2500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP260 is connected to a high-voltage power source when the test circuit is activated.

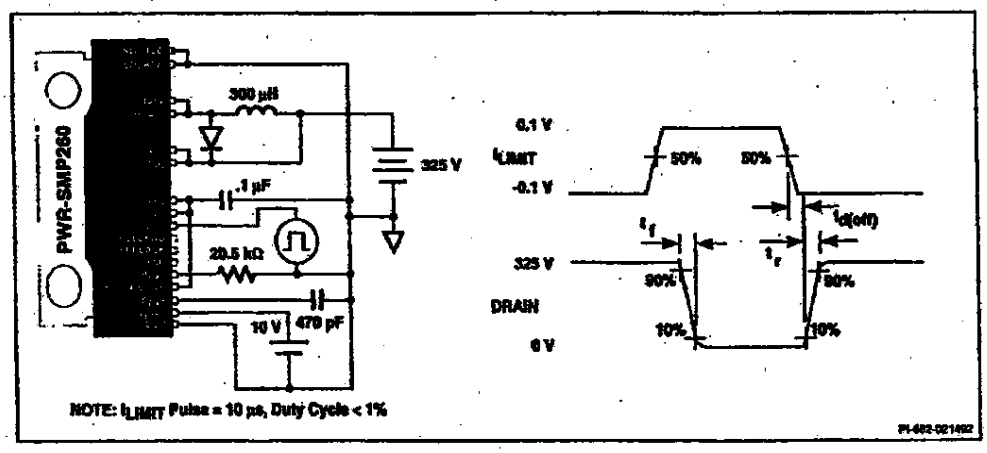
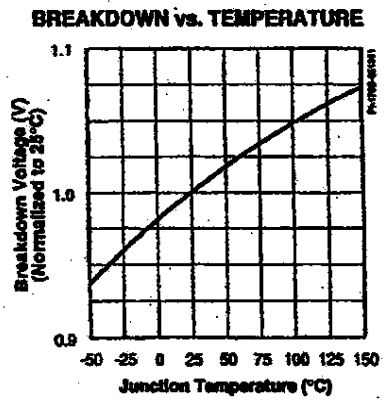
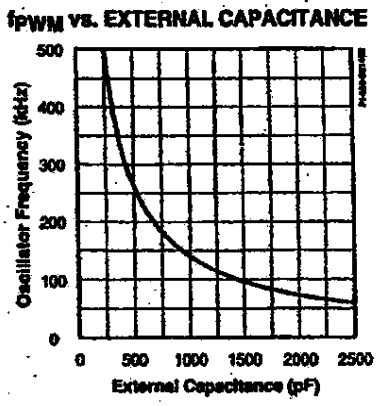
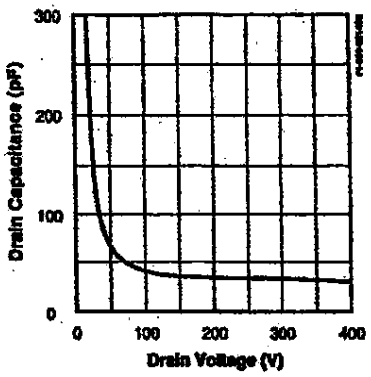


Figure 8. Switching Time Test Circuit.

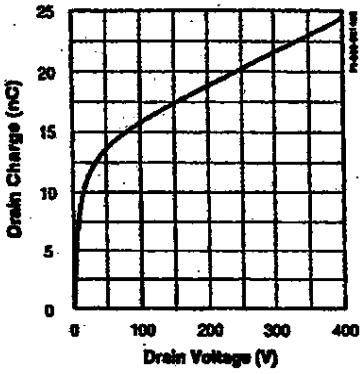




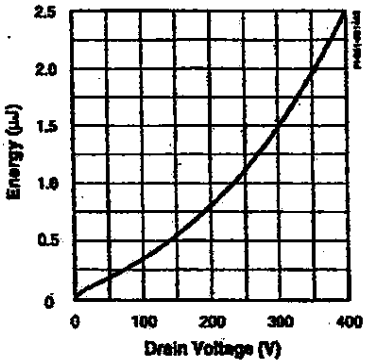
C_{OSS} vs. DRAIN VOLTAGE



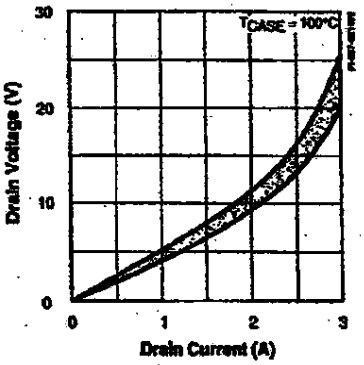
DRAIN CHARGE vs. DRAIN VOLTAGE



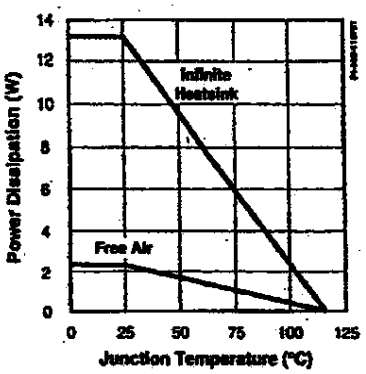
DRAIN CAPACITANCE ENERGY



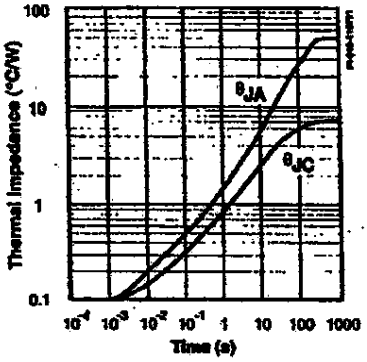
TRANSFER CHARACTERISTICS



PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



DX 76

SMP211

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 10 W from rectified 220 VAC input, 5 W from rectified universal (85 to 265 VAC) input
- External transformer provides isolated output voltages
- Integrated solution minimizes overall size

High-voltage, Low-capacitance MOSFET Output
- Designed for 120/220 V off-line applications
- Can also be used with DC inputs from 36 V to 400 V
- Low capacitance allows for high frequency operation

High-speed Voltage-mode PWM Controller
- Internal pre-regulator self-powers the IC on start-up
- Wide V_{BIAS} voltage range
- Designed for use with optocoupler feedback

Built-In Self-protection Circuits
- Adjustable cycle-by-cycle current limit
- Latching shutdown can be used for output overvoltage protection
- Input undervoltage lockout
- Thermal shutdown

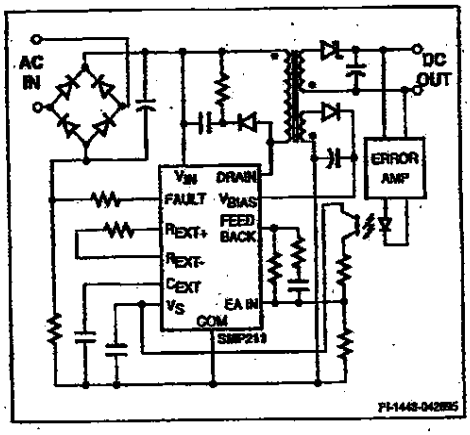


Figure 1. Typical Application

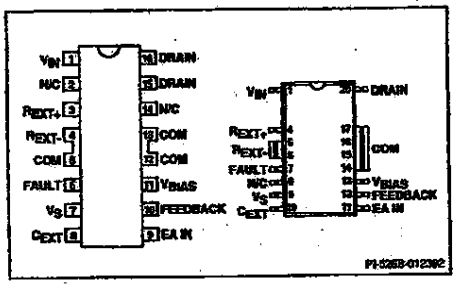


Figure 2. Pin Configuration

Description

The SMP211, intended for 220 V or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a small, low-cost, isolated, off-line power supply.

The high-speed power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low threshold voltage. Low capacitance and low threshold voltage reduce gate drive and bias power, allowing higher frequency operation.

The controller section of the SMP211 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, error amplifier, gate driver, and circuit protection. This voltage-mode Pulse Width Modulation control circuit is optimized for flyback topologies, but may be used with other topologies as well.

The SMP211 is available in a 16-pin plastic batwing DIP or 20-pin batwing SOIC package.

PART NUMBER	PACKAGE OUTLINE	T_J RANGE
SMP211BNI	P16B	-40 to 125°C
SMP211SRI	S20B	-40 to 125°C

TOP200 FAMILY RECOMMENDED FOR NEW DESIGNS

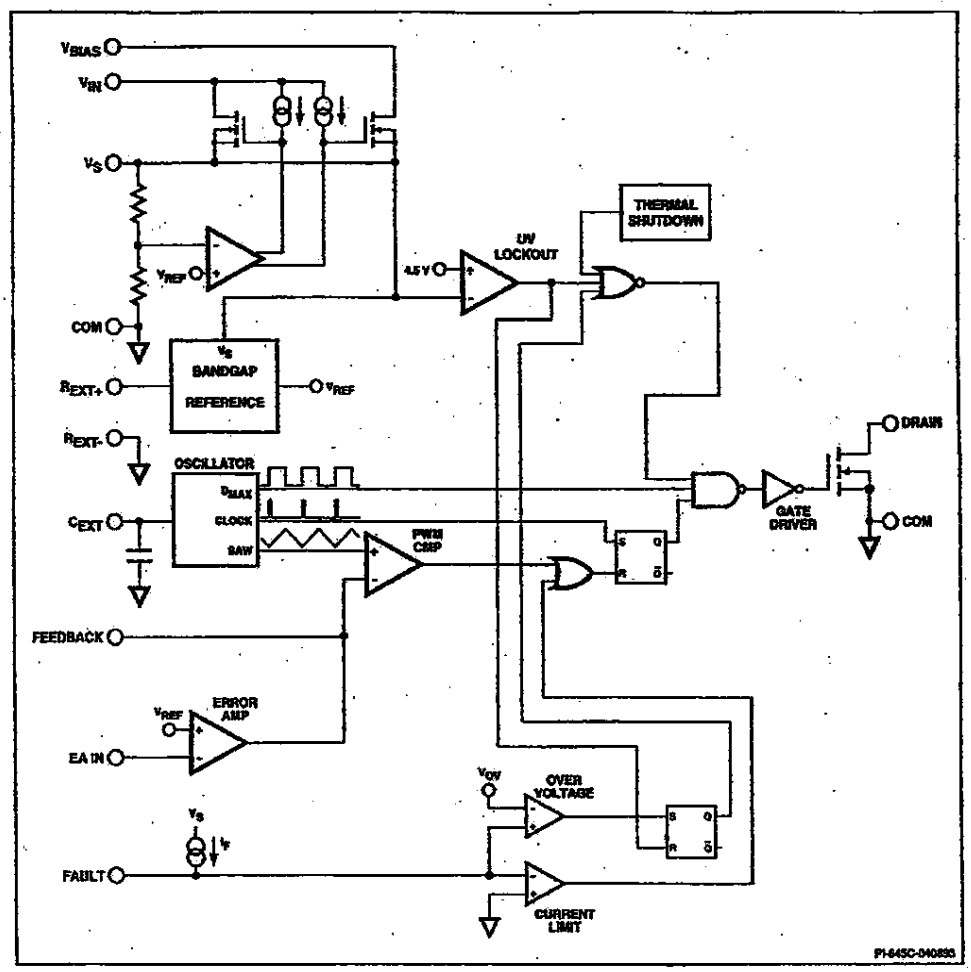


Figure 3. Functional Block Diagram of the SMP211.

2

Pin Functional Description

(Pin Number in Parentheses for SOIC version)

Pin 1(1):
High voltage V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 2:
N/C for creepage distance.

Pin 3(4):
A resistor placed between R_{EXT+} and R_{EXT-} sets the internal bias currents.

Pin 4(5, 6):
R_{EXT-} is the return for the reference current.

Pin 5, 12, 13(14, 15, 16, 17):
COM connections. Ground or reference point for the circuit.

Pin 6(7):
The FAULT pin is used with an external resistor to implement current limit. This pin may also driven by an optocoupler to implement over voltage protection of the power supply output.

Pin 7(9):
Connection for a bypass capacitor for the internally generated V_S supply.

Pin 8(10):
C_{EXT} is used to set the oscillator frequency. Adding external capacitance lowers the PWM frequency.

Pin 9(11):
EA IN is the error amplifier inverting input for connection to the external feedback and compensation networks.

Pin 10(12):
FEEDBACK is the error amplifier output for connection to the external compensation network.

Pin 11(13):
V_{BIAS} is the bootstrap voltage used to self-power the device once the supply is operating.

Pin 14:
N/C for creepage distance.

Pin 15, 16(20):
Open DRAIN of the output MOSFET. Both pins must be externally connected.

SMP211 Functional Description

2

Bias Regulator
The onboard supply voltage (V_S) is supplied from either of two high-voltage linear regulators. The V_{IN} linear regulator draws current from the high-voltage bus while the V_{BIAS} regulator draws current from a voltage generated from a transformer winding. The V_{IN} regulator dissipates significant power levels and should be cut off during normal operation for improved efficiency. The V_S error amplifier has a built-in preference for generating V_S from the V_{BIAS} regulator, which automatically cuts off the V_{IN} regulator during normal operation. During start-up and under power supply fault conditions, the bias error amplifier generates V_S from the V_{IN} regulator.

V_S is the supply voltage for the controller and driver circuitry. An external bypass capacitor connected to V_S is required for filtering and noise immunity. The value of V_S also determines when the internal undervoltage lockout is enabled. Undervoltage lockout disables the power MOSFET until V_S is within its normal operating range.

Bandgap Reference
V_{REF} is a 1.25 V reference voltage generated by the temperature compensated bandgap reference. This reference voltage is used for setting thresholds for comparators, amplifiers, and the thermal shutdown circuit. The external resistor connected between R_{EXT+} and R_{EXT-} and the bandgap reference set the proper internal bias current levels for the various internal circuits.

Oscillator
The oscillator linearly charges and discharges the combined internal and external capacitance between two different voltage levels to create a sawtooth waveform for the pulse width modulator. Two digital signals, D_{MAX} and CLOCK are also generated. D_{MAX} corresponds to the rising portion of the sawtooth waveform, and is used to gate the MOSFET driver. A short CLOCK pulse is used to reset the pulse width modulation and current limit latch at the beginning of each cycle.

SMP211 Functional Description (cont.)

Error Amplifier
The error amplifier consists of a high performance operational amplifier with the non-inverting input connected to the internal bandgap reference voltage. The output of the error amplifier directly controls the duty cycle of the power switch.

Pulse Width Modulator
The pulse width modulator implements a voltage-mode control loop by driving the power MOSFET with a duty cycle proportional to the voltage on the FEEDBACK pin as shown in Figure 4. The duty cycle signal is generated by a comparator which compares the FEEDBACK voltage with the sawtooth waveform generated on the C_{osc} pin. As the input voltage increases the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the power MOSFET. The pulse width modulator resets the latch, turning off the power MOSFET. The D_{MAX} signal from the oscillator limits the maximum duty cycle by gating the output driver.

Fault Protection
The FAULT pin is used to implement both cycle-by-cycle MOSFET transistor current limiting and latching output shutdown protection.

The FAULT pin turns off the power MOSFET switch when an overcurrent condition causes the voltage on this pin to drop below the FAULT current limit threshold. The DRAIN current is converted to a voltage by an external sense resistor. An internal current source applied to an external offset resistor biases the FAULT signal to a positive voltage when no DRAIN current is flowing. During an overcurrent condition, current flowing in the sense resistor will cause the FAULT voltage to decrease. When the FAULT voltage falls below the fault current limit threshold for a time period exceeding the current limit delay, the power switch will be latched off until the beginning of the next clock cycle as shown in Figure 4. The FAULT pin will continuously limit the duty cycle on a cycle-by-cycle basis until the fault condition is removed.

For latching output overvoltage protection, an external optocoupler can be used to drive the FAULT pin above the FAULT OV threshold, as shown in Figure 5. A latch is set that turns off the power MOSFET switch. Cycling the undervoltage lockout circuit by removing and restoring input power is necessary to reset the latch and resume normal power supply operation.

Overtemperature Protection
Temperature protection is provided by a precision analog circuit that turns the power switch off and reduces supply current when the switch junction gets too hot (typically 140°C). When the circuit has cooled past the hysteresis temperature, normal operation resumes.

General Circuit Operation

The flyback power supply circuit shown in Figure 6 is a 5 volt, 5 watt power supply that operates from 85 to 265 V(rms) AC input voltage. The output voltage is directly sensed and accurately regulated by a secondary-referenced error amplifier. The error amplifier drives an error signal through an optocoupler to the SMP211 which directly controls the duty cycle of the integrated high voltage MOSFET switch. The effective output voltage can be fine-tuned by adjusting the resistive divider formed by R13 and R14. Other output voltages are possible by adjusting the transformer turns ratios as well as the resistor divider.

AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high voltage MOSFET transistor within the SMP211. The clamp circuit implemented by R10, C9, and D5 clamps the leading edge voltage spike caused by transformer leakage inductance to a safe value. Ringing caused by parasitic capacitance and leakage inductance is damped by C15 and R9. The power secondary winding is rectified and filtered by D2, C2, and C10 to create the desired output voltage. The bias winding is rectified and filtered by D3 and C5 to create a bias voltage to the SMP211 which effectively cuts off the high voltage internal linear regulator. Common-mode emission currents which flow between the primary windings of the transformer and the secondary output circuitry are attenuated by C12, C17, C7, C8, L2, and L4. Differential-mode emission currents caused by pulsating currents at the input of the power supply are attenuated by C6 and L3. Voltage spikes on the AC line are clamped by VR1.

Internal bias currents are accurately set by R3. Bypass capacitor C3 filters current spikes on the internally generated voltage source V_s. The oscillator frequency is determined by C11.

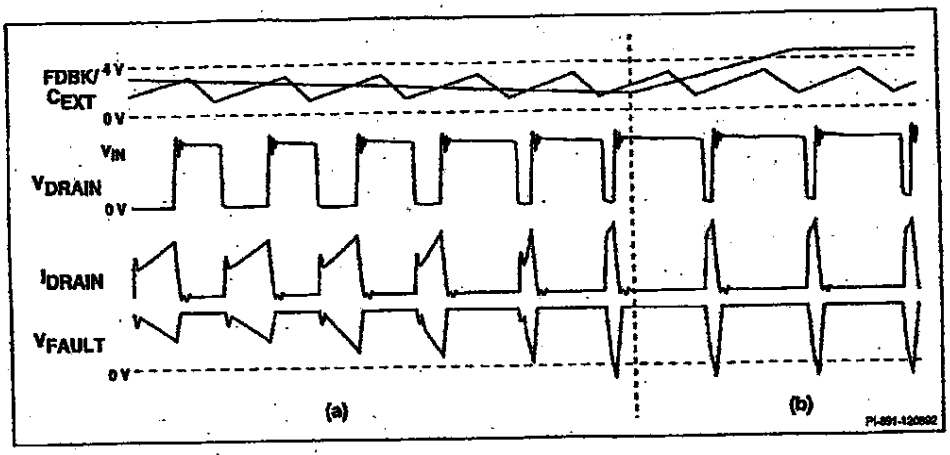


Figure 4. Typical Waveforms for (a) Normal Operation, and (b) Cycle-by-cycle Current Limit.

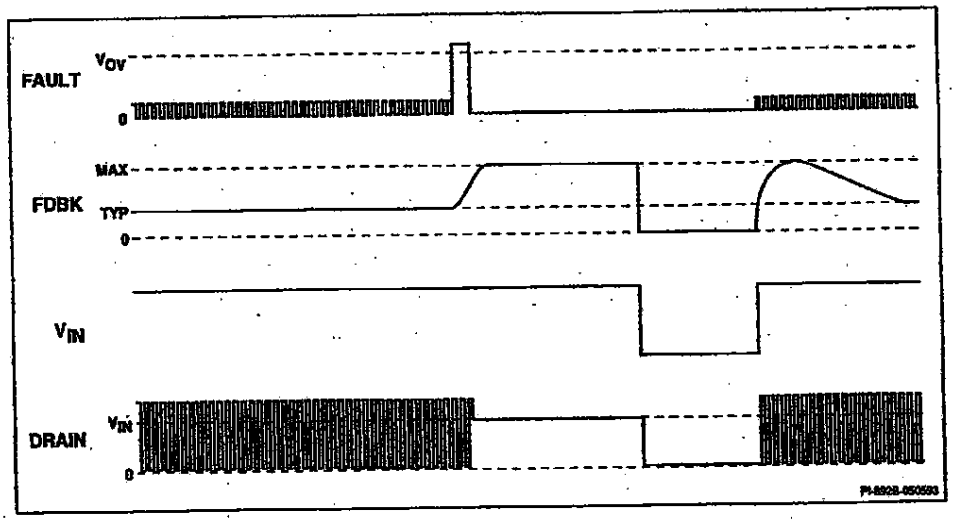


Figure 5. Typical Waveforms for Overvoltage Shutdown.

5 W Universal Off-line Power Supply with Optocoupler Feedback

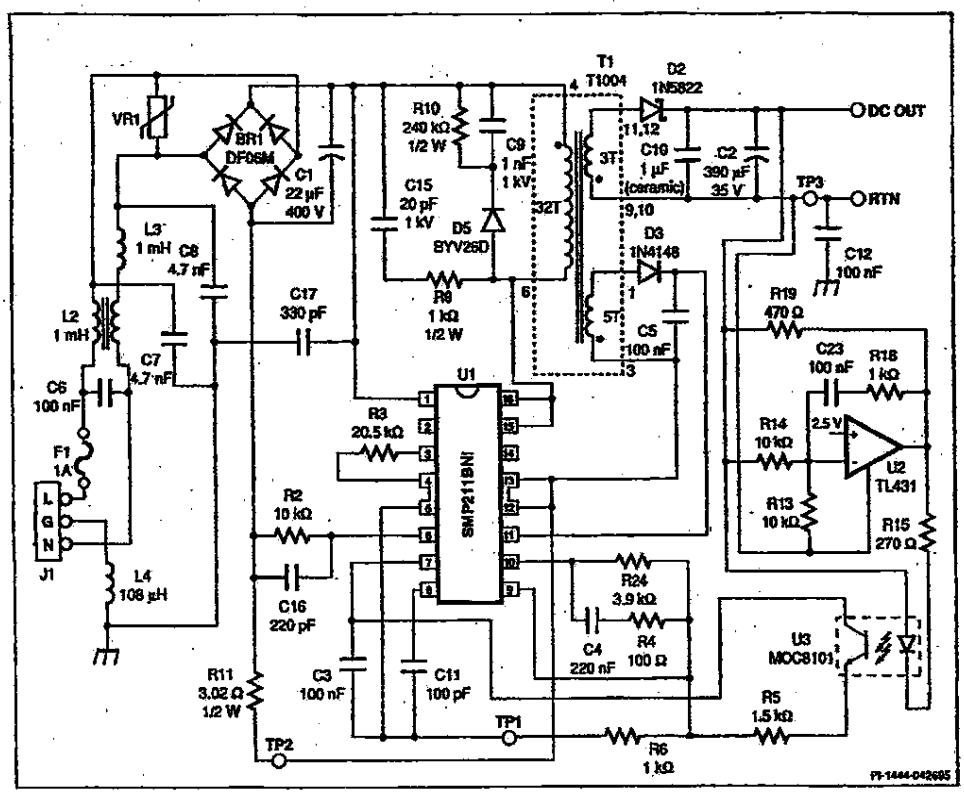


Figure 6. Schematic Diagram of a 5 V, 5 W Universal Input Power Supply Utilizing the SMP211 with Optocoupler Feedback.

2

General Circuit Operation (cont.)

Transistor switch current is sensed by R11. The initial voltage level at the FAULT pin is determined by R2. C16 filters drain switching noise without delaying the current sense signal across R11.

The secondary-referenced error amplifier control system is implemented with a TL431 shunt regulator (U2). This device consists of an accurate 2.5 V bandgap reference, error amplifier, and driver. The output voltage is sensed, divided by R13 and R14, and applied to the inverting input of the error amplifier. The non-inverting input of the error amplifier is internally connected to the bandgap reference voltage. The frequency response of the error amplifier is determined by the compensation network consisting of R18, C23, and the high frequency gain setting resistor R14. Bias current of 2 mA minimum for U2 is provided by R19. The LED current in the optocoupler is limited by R15.

To achieve full output power and reliable operation of the SMP211, both DRAIN outputs on the plastic batwing DIP version must be connected together at the printed circuit board. These pins are not connected within the package.

To reduce device power dissipation and temperature rise during normal operation, the voltage applied to V_{BIAS} must be greater than the minimum specified value to ensure complete cutoff of the high-voltage linear regulator. Ensure that the maximum specified

General Circuit Operation (cont.)

voltage on the V_{BIAS} pin is not exceeded when adjusting the value of the output voltage.

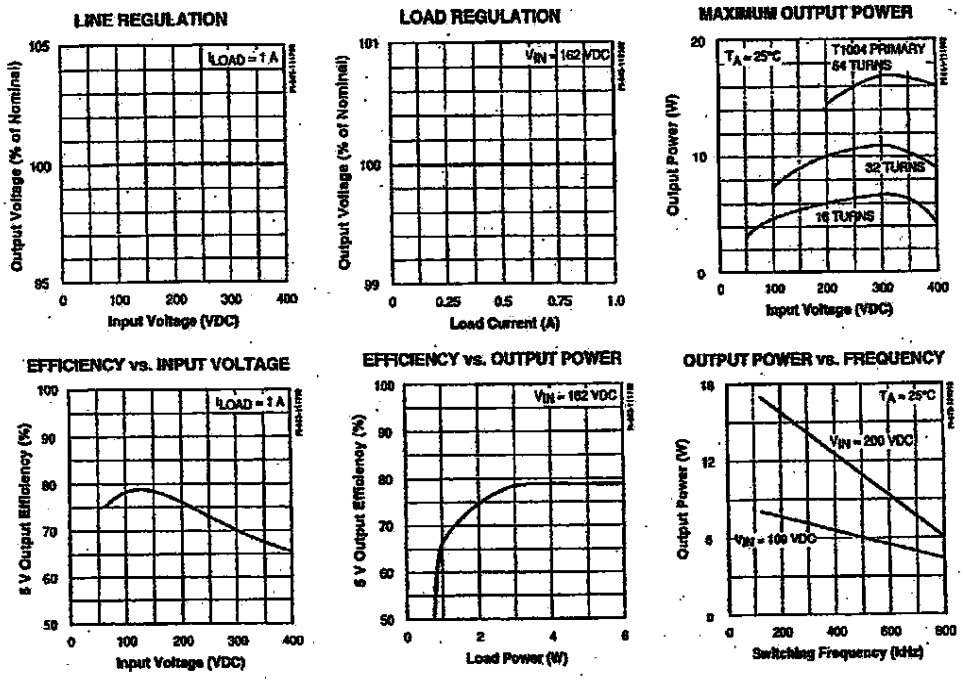
Performance data is shown below for the power supply circuit given in Figure 6.

The line and load regulation graphs were measured when operated from a DC source. The switching frequency of the power supply was measured at 250 kHz.

The maximum output power curve shows the power output capability for the normal transformer, and the performance with twice and half the normal number of primary turns.

The output power versus frequency curve was generated by characterization of the SMP211 at various frequencies. Several different power transformers, optimized for each frequency, were used to generate the maximum power at each point. The curves illustrate the trade-off between AC and DC power losses within the device. As AC losses rise with frequency, DC losses and output power must be reduced to maintain the same device maximum power dissipation.

Typical Performance Characteristics (Figure 6 Power Supply)



Upgrading Existing SMP210 Designs to the SMP211

The SMP211 is compatible with PC boards designed for the SMP210. The resistor required between V_S and I_{LIMIT} on the SMP210 has been eliminated on the SMP211. The I_{LIMIT} pin on the SMP210 has been renamed to FAULT on the SMP211 due to the additional overvoltage protection feature. External resistor R2 will have a different value when using the SMP211.

EA- and EAO on the SMP210 have been renamed EA IN and FEEDBACK on the SMP211 because the use of the internal error amplifier is optional. When using primary-referenced feedback winding control the functionality is the same for both devices. An example of this method using the SMP211 is shown in Figure 7.

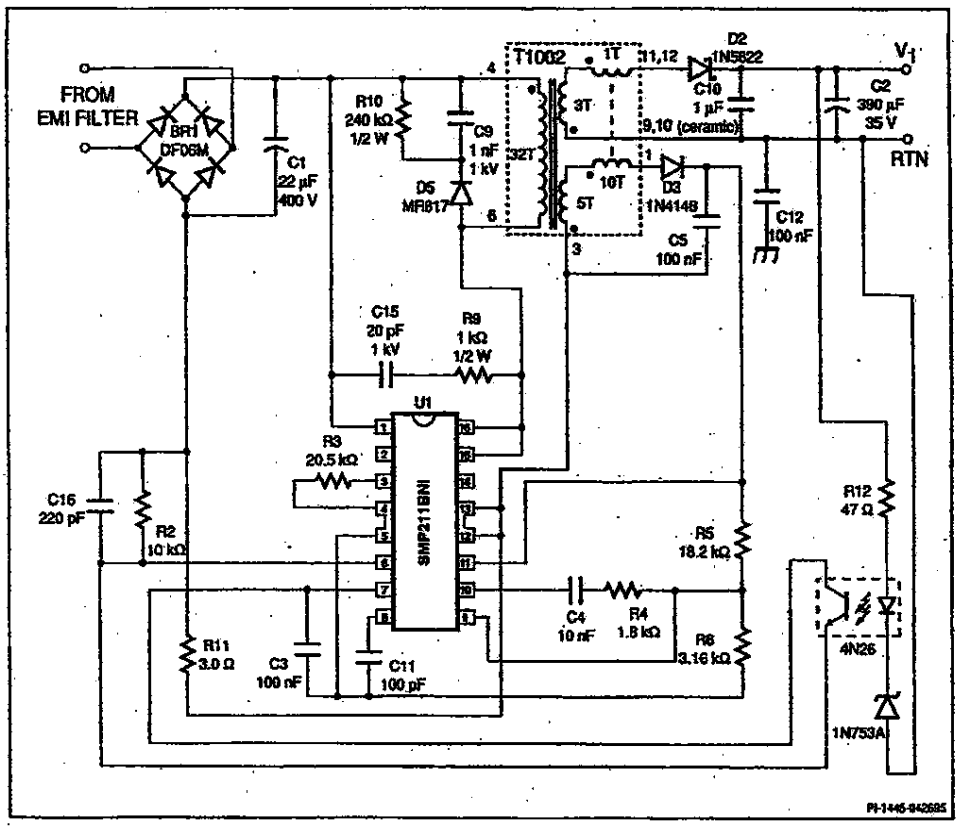


Figure 7. Implementing Feedback Winding Regulation and Output Overvoltage Protection.

Implementing Output Overvoltage Protection

If the load is extremely sensitive to overvoltage conditions, an overvoltage shutdown function can be implemented as shown in Figure 7. The output voltage is fed back to the SMP211 via an op amp and optocoupler. If the voltage at pin 6 is greater than V_{OV}, the internal latch will shut off the output.

The SMP211 must be restarted by removing the input voltage and then reapplying it, causing the latch to reset and the circuit to begin a new startup cycle.

Drain Voltage	800 V
V_{IN} Voltage	500 V
V_{BIAS} Voltage	35 V
Drain Current[2]	800 mA
Input Voltage[3]	- 0.3 V to V_S + 0.3 V
Storage Temperature	-65 to 125°C
Operating Junction Temperature[4]	-40 to 150°C
Lead Temperature[5]	260°C
Power Dissipation	
BN Suffix (T_A = 25°C)	2.33 W
(T_A = 70°C)	1.28 W
SR Suffix (T_A = 25°C)	3.33 W
(T_A = 70°C)	1.83 W
Thermal Impedance (θ_{JA}) (BN Suffix)	43°C/W
(SR Suffix)	30°C/W
Thermal Impedance (θ_{JC})[6] (BN Suffix)	6°C/W
(SR Suffix)	6°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 300 µs, 2% duty cycle.
3. Does not apply to V_{IN} or DRAIN.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Measured at pin 12/13 (BN Suffix), or pin 15/16 (SR Suffix).

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_{EXT} = 100 pF, T_J = -40 to 125°C (See Note 1)	Min	Typ	Max	Units
Output Frequency	f_{osc}	C_{EXT} = Open		900		kHz
			193	233	272	
Duty Cycle Range	DC	C_{EXT} = Open	0-35	0-40		%
			0-48	0-52		
FAULT Offset Current	I_F		-103	-93	-83	µA
FAULT OV Threshold	V_{OV}		3.5	V_S-1.6 V	4.9	V
FAULT Current Limit Threshold	V_{ILIMIT}		-100		0	mV
Current Limit Delay Time	$t_{d(off)}$	See Figure 8	75	150	250	ns
Thermal Shutdown Temperature			125	140		°C
Thermal Shutdown Hysteresis				15		°C

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V, R_{EXT} = 20.5 kΩ, C_{EXT} = 100 pF, T_j = -40 to 125°C (See Note 1)		Min	Typ	Max	Units
Reference Voltage	V_{REF}			1.21	1.25	1.29	V
Reference Voltage Temperature Drift	ΔV_{REF}				±300		ppm/°C
Gain-Bandwidth Product					500		kHz
DC Gain	A_{VOL}			60	80		dB
Output Current	I_{OUT}	V_{FB} = 2.3 V			-2.5		mA
		V_{FB} = 1.1 V			0.7		
Output Impedance	Z_{OUT}				27		Ω
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C		20	25	Ω
			T_j = 100°C		33	43	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V	T_j = 25°C	300	380		mA
			T_j = 100°C	200	240		
OFF-State Current	I_{DSS}	V_{DRAIN} = 640 V, T_A = 125°C			100	500	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 250 µA, T_A = 25°C		800			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			45		pF
Output Stored Energy	E_{OSS}	V_{DRAIN} = 400 V			700		nJ
Rise Time	t_r	See Figure 8			70	150	ns
Fall Time	t_f	See Figure 8			70	150	ns

2

Parameter	Symbol	Conditions (Unless Otherwise Specified) V_{IN} = 325 V, V_{BIAS} = 8.5 V, COM = 0 V R_{EXT} = 20.5 kΩ, C_{EXT} = 100 pF T_J = -40 to 125°C (See Note 1)	Min	Typ	Max	Units
Pre-regulator Voltage	V_{IN}		36		500	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected, C_{EXT} = Open		3	4.5	mA
		V_{BIAS} > 8.25 V			0.1	
		Thermal Shutdown ON			2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied	8.25		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied		3	4.5	mA
V_S Source Voltage	V_S		5.1		6.4	V
V_S Source Current	I_S				5	mA

NOTES:

1. Applying >3.5 V to the C_{EXT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the SMP211 is connected to a high voltage power source when the test circuit is activated.

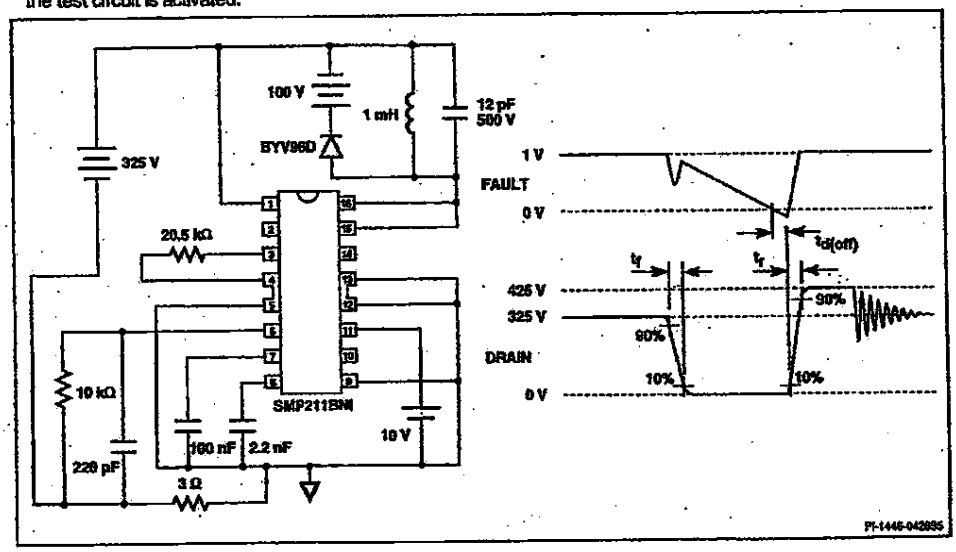
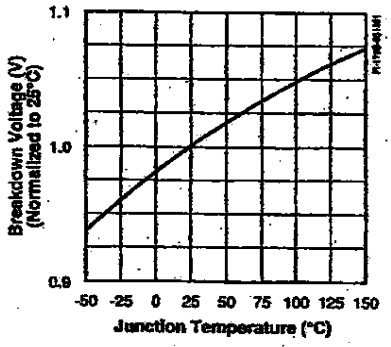
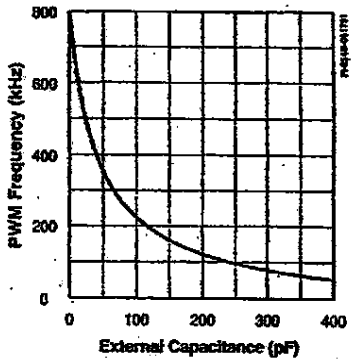


Figure 8. Current Limit Delay/Switching Time Test Circuit.

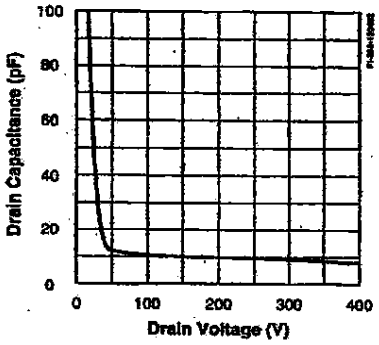
BREAKDOWN vs. TEMPERATURE



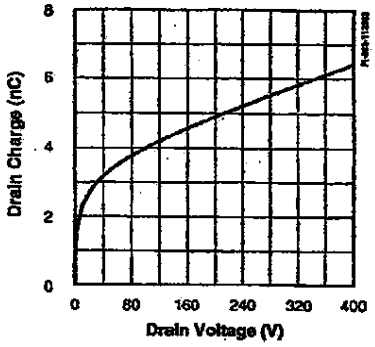
f_{PWM} vs. EXTERNAL CAPACITANCE



C_{OSS} vs. DRAIN VOLTAGE



DRAIN CHARGE vs. DRAIN VOLTAGE



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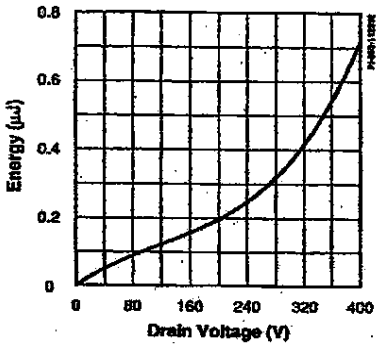
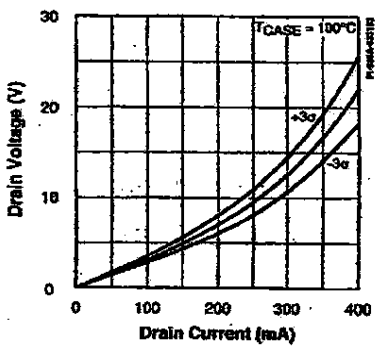
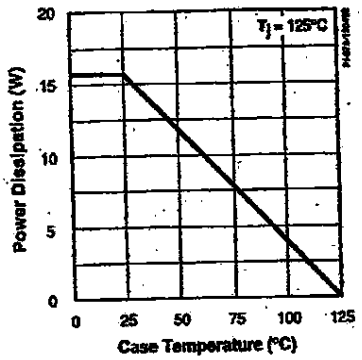
DRAIN CAPACITANCE ENERGY



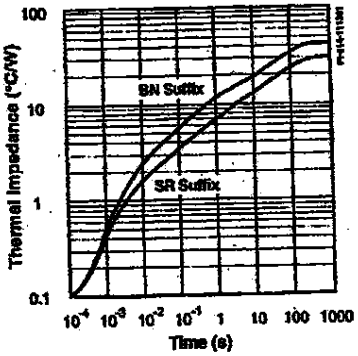
OUTPUT CHARACTERISTICS



PACKAGE POWER DERATING

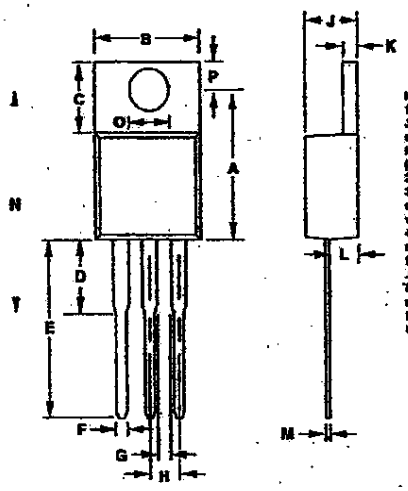


TRANSIENT THERMAL IMPEDANCE



2

A	.460-.489	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.15
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87



Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (Issue J, March 1987)
2. Controlling dimensions are inches.
3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
6. All terminals are solder plated.

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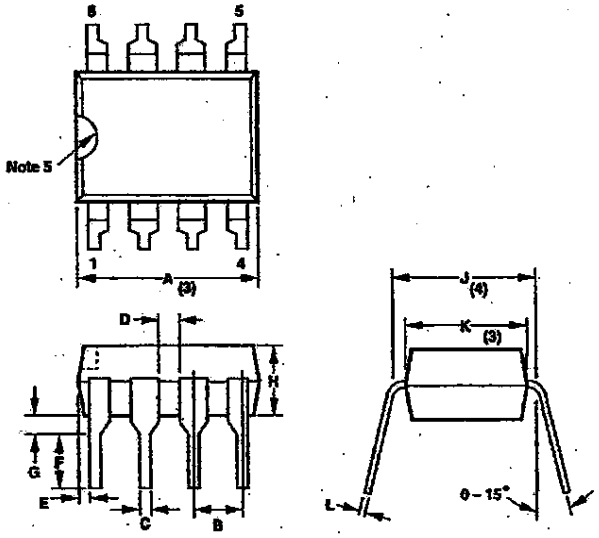
A	.395 MAX	10.03 MAX
B	.090-.110	2.29-2.79
C	.015-.021	0.38-0.53
D	.040 TYP	1.02 TYP
E	.015-.030	0.38-0.76
F	.125 MIN	3.18 MIN
G	.015 MIN	0.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	0.23-0.38



Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (Issue B, 7/85).
2. Controlling dimensions: inches.
3. Dimensions are for the molded body and do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

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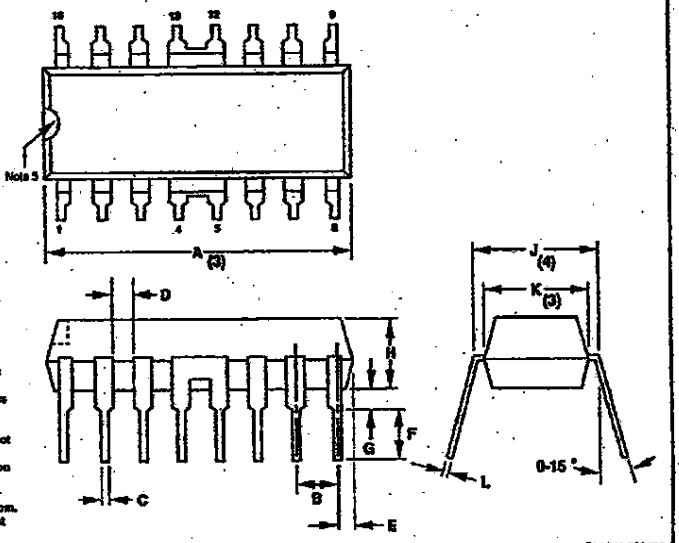
PACKAGES

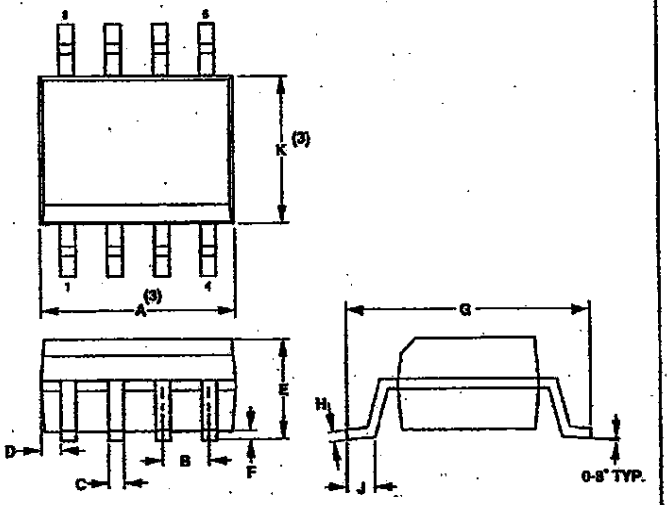
A	.780 MAX	19.81 MAX
B	.090-.110	2.29-2.79
C	.015-.021	.38-.53
D	.040 TYP	1.02 TYP
E	.015-.030	.38-.76
F	.125 MIN	3.18 MIN
G	.015 MIN	.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	.23-.38



Notes:
1. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 18 leads (issue B, 7/85). Except for joining of Pins 4-5 and Pins 12-13.
2. Controlling dimension: inches.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

PI-1844-050196

A	0.189-0.197	4.80-5.00
B	0.050 TYP	1.27 TYP
C	0.014-0.019	0.35-0.49
D	0.012 TYP	0.31 TYP
E	0.053-0.069	1.35-1.75
F	0.004-0.010	0.10-0.25
G	0.228-0.244	5.80-6.20
H	0.007-0.010	0.19-0.25
J	0.021-0.045	0.51-1.14
K	0.150-0.157	3.80-4.00



Notes:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75 mm (.150 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .25 mm (.006 inch) on any side.
4. Pin 1 side identified edge by chamfer on top of the package body or indent on Pin 1 end.

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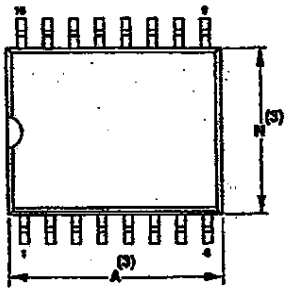
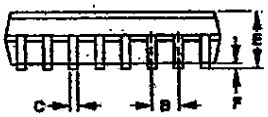
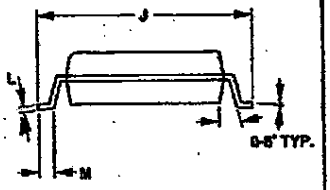
7289229 0001811 558

A	.398-.413	10.10-10.50
B	.050 BSC	1.27 BSC
C	.014-.018	0.36-0.46
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.418	10.01-10.62
L	.009-.012	0.23-0.32
M	.020-.040	0.51-1.02
N	.291-.299	7.40-7.60

Notes:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50 mm (.300 inch) body width (Issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.



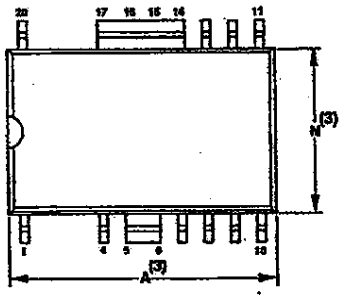


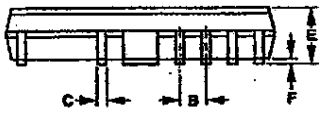


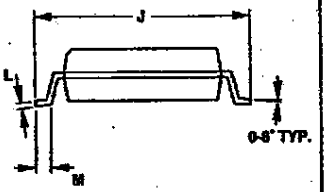
PI-1846-050196

A	.496-.512	12.60-13.00
B	.050 BSC	1.27 BSC
C	.014-.019	0.35-0.49
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.419	10.00-10.65
L	.009-.013	0.23-0.32
M	.016-.050	0.40-1.27
N	.291-.299	7.40-7.60

Notes:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 28 leads, 7.50 mm (.300 inch) body width (Issue A, June 1985). Except for joining of Pins 8-8 and Pins 15-14-16.
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.







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Tape & Reel Ordering Information

Power Integrations, Inc. makes selected surface-mount parts available in tape and reel form for use with automatic pick-and-place equipment. Tape and reel specifications meet or exceed industry standard specification EIA-481.

Ordering Information

Parts available in tape and reel form can be ordered by placing a T&R ordering suffix after the base part number. Standard orientation is Pin 1 Left. The ordering suffix for this orientation (see Figure 1) is TL. For example:

Base Part #	T&R Suffix
INT100S	-TL

Please contact the factory for other options. Minimum order size is 1 reel per line item, and all orders will be in multiples of full reel quantities. The quantity per reel for each package type is shown in Table 1. Power Integrations normal terms and conditions apply.

Electrical Specifications

Parts are subjected to the Power Integrations standard test flow, after which the parts are loaded into the tape cavities and sealed with a cover tape using standard anti-static handling procedures. The tape and cover are constructed of conductive modified polystyrene, providing a surface resistivity of $\leq 10^5$ Ω/square. The reel is made of polystyrene with a topical anti-static coating, providing a surface resistivity of $\leq 10^{11}$ Ω/square.

Physical Specifications

Physical specifications of the tape, cover, and reel are governed by EIA-481. Physical dimensions of the tapes are given in Figure 2 and Table 2, and physical dimensions of the reels are given in Figure 3 and Table 3.

Packaging for Shipment

Power Integrations supplies the following information on the side of each reel for ease of product identification:

- Power Integrations part number (MPN), including orientation suffix
- Encapsulation date code (D/C)
- Assembly lot identification (LOT)
- Quantity (QTY)
- Tape and reel packing date code (R/D)

SO-8	12mm	8mm	330mm	2500
SO-16 (W)	16mm	12mm	360mm	1000
SO-20	24mm	12mm	360mm	1000

Table 1. Primary Tape & Reel Dimensions and Reel Quantities.

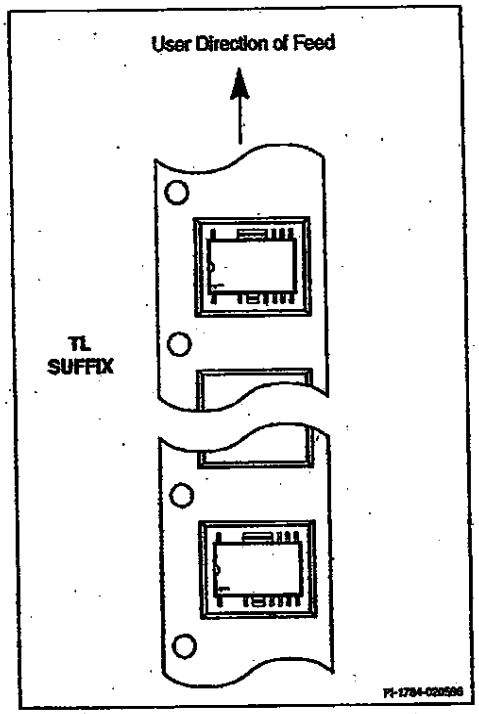

Figure 1. Part Orientation and Ordering Suffix.

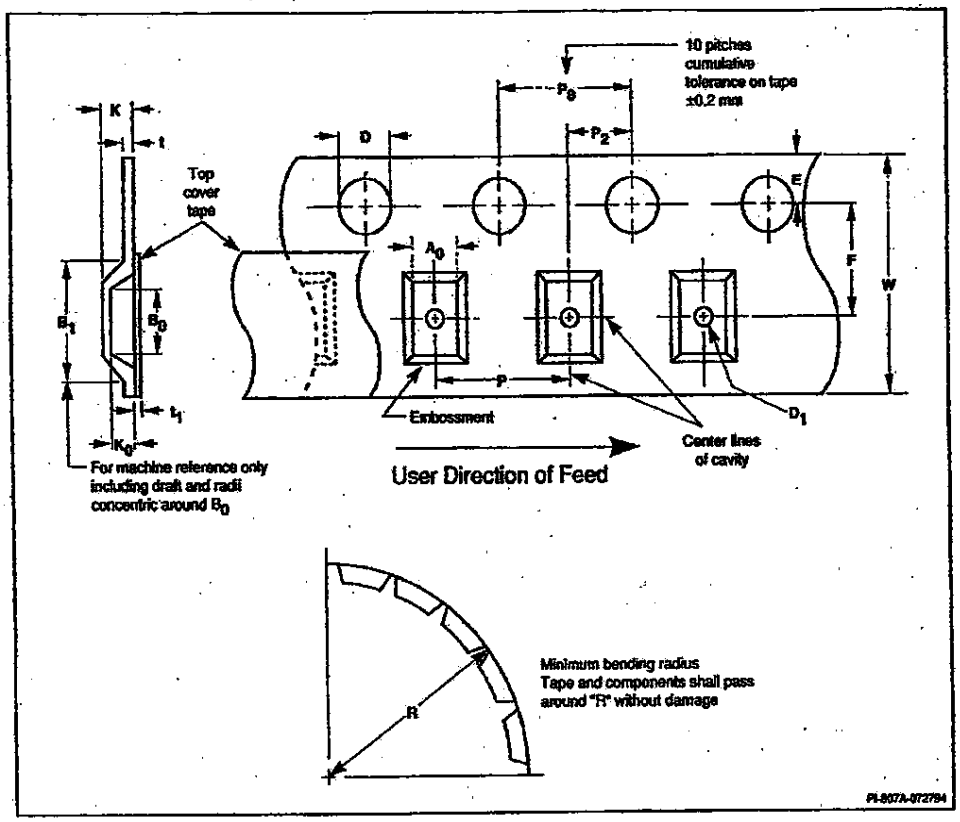

Figure 2. Tape Dimension Index.

Plastic SO-8	12 mm	6.3-6.5	5.1-5.3	8.2 (max)	1.5-1.6	1.5 (min)	1.65-1.85	5.45-5.55	4.5 (max)
Plastic SO-16 (W)	16 mm	10.8-11.0	10.6-10.8	12.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	7.40-7.60	6.5 (max)
Plastic SO-20	24 mm	10.8-11.0	13.2-13.4	20.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	11.40-11.60	6.5 (max)

Plastic SO-8	12 mm	2.00-2.20	7.9-8.1	3.9-4.1	1.95-2.05	30 (min)	0.400 (max)	0.10 (max)	11.7-12.3
Plastic SO-16 (W)	16 mm	2.90-3.10	11.9-12.1	3.9-4.1	1.90-2.10	40 (min)	0.400 (max)	0.10 (max)	15.7-16.3
Plastic SO-20	24 mm	2.90-3.10	11.9-12.1	3.9-4.1	1.90-2.10	50 (min)	0.400 (max)	0.10 (max)	23.7-24.3

Table 2. Tape Dimensions (in mm).

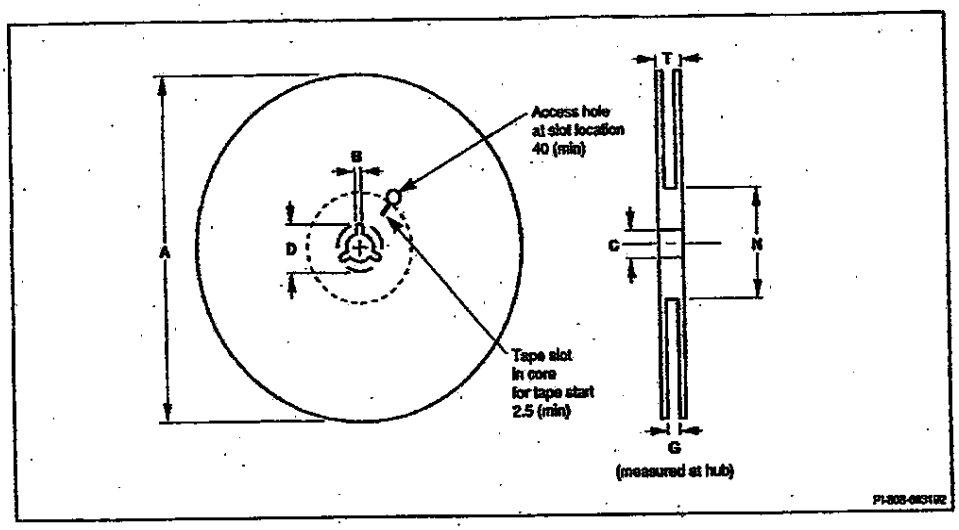

Figure 3. Reel Dimension Index.

Plastic SO-8	12 mm	330 (max)	1.5 (min)	12.80-13.20	20.2 (min)	12.4-14.4	50 (min)	18.4 (max)
Plastic SO-16 (W)	16 mm	360 (max)	1.5 (min)	12.80-13.20	20.2 (min)	16.4-18.4	50 (min)	22.4 (max)
Plastic SO-20	24 mm	360 (max)	1.5 (min)	12.80-13.20	20.2 (min)	24.4-26.4	50 (min)	30.4 (max)

Table 3. Reel Dimensions (in mm).

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DX 77

REDACTED

DX 89

United States Patent [19]

Colak

[11] Patent Number: 4,626,879

[45] Date of Patent: Dec. 2, 1986

[54] LATERAL DOUBLE-DIFFUSED MOS TRANSISTOR DEVICES SUITABLE FOR SOURCE-FOLLOWER APPLICATIONS

[75] Inventor: Sel Colak, Ossining, N.Y.

[73] Assignee: North American Philips Corporation, New York, N.Y.

[21] Appl. No.: 766,665

[22] Filed: Aug. 15, 1985

Related U.S. Application Data

[63] Continuation of Ser. No. 451,993, Dec. 21, 1982, abandoned.

[51] Int. Cl.[4] H01L 29/94

[52] U.S. Cl. 357/23.4; 357/23.8; 357/23.14; 357/13

[58] Field of Search 357/23.4, 23.8

[56] References Cited

U.S. PATENT DOCUMENTS

4,292,642	9/1981	Appels et al.	357/13
4,300,150	11/1981	Colak	357/13
4,422,089	12/1983	Vaes et al.	357/23.4

OTHER PUBLICATIONS

Pocha et al, "Tradeoff Between Threshold Voltage and Breakdown in High Voltage Double-Diffused MOS Transistors", *IEEE Trans. on Elec. Dev.*, vol. ED25, No. 11, Nov. 1978.

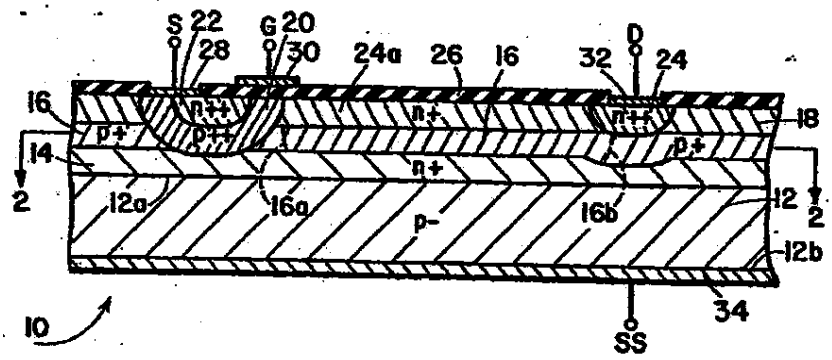
Colak et al., "Lateral DMOS Power Transistor Design", *IEEE Electron Device Letters*, vol. EDL-1, No. 4, Apr. 80.

Primary Examiner—Martin H. Edlow
Assistant Examiner—Charles S. Small, Jr.
Attorney, Agent, or Firm—Robert T. Mayer; Steven R. Biren

[57] ABSTRACT

A lateral double-diffused MOS transistor includes an intermediate semiconductor layer of the same conductivity type as the channel region which extends laterally from the channel region to beneath the drain contact region of the device. This intermediate semiconductor layer substantially improves the punchthrough and avalanche breakdown characteristics of the device, thus permitting operation in the source-follower mode, while also providing a compact structure which features a relatively low normalized "on" resistance.

12 Claims, 5 Drawing Figures



Case No. 04-1371-JJF
DEFT Exhibit No. DX 89
Date Entered _____
Signature _____

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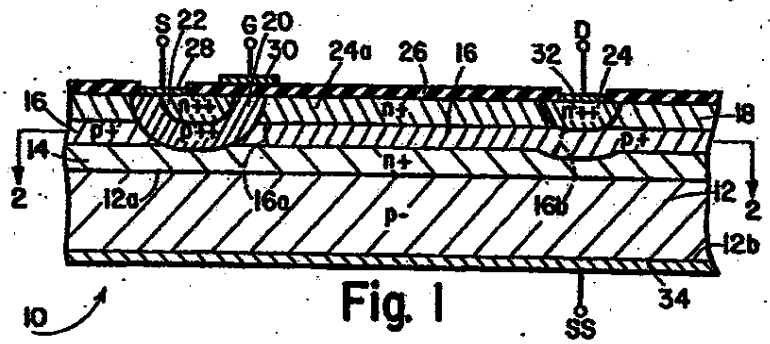

Fig. 1

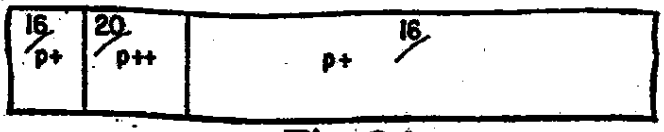

Fig. 2A

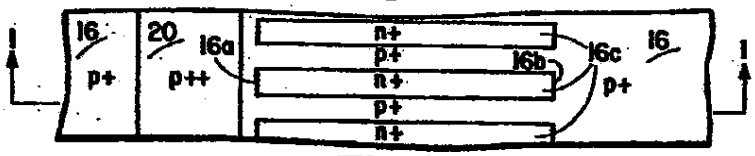

Fig. 2B

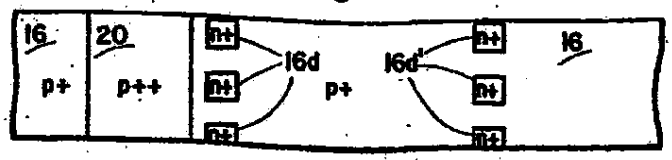

Fig. 2C

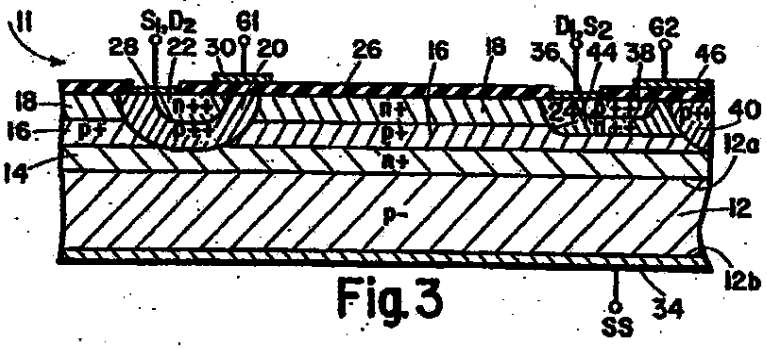

Fig. 3

LATERAL DOUBLE-DIFFUSED MOS TRANSISTOR DEVICES SUITABLE FOR SOURCE-FOLLOWER APPLICATIONS

This is a continuation of application Ser. No. 451,993, filed Dec. 21, 1982, now abandoned.

BACKGROUND OF THE INVENTION

The invention is in the field of metal-oxide-semiconductor (MOS) field-effect devices, and relates specifically to lateral double-diffused MOS (DMOS) field-effect transistors suitable for use in source-follower applications.

A typical prior-art high voltage DMOS transistor is shown on page 1325 of the "IEEE Transactions on Electron Devices", Vol. ED-25, No. 11, November 1978, in a paper entitled "Tradeoff Between Threshold Voltage and Breakdown in High-Voltage Double-Diffused MOS Transistors", by Pocha et al. This device includes a semiconductor substrate of a first conductivity type (p-type), a surface layer of a second conductivity type (n-type) on the substrate, a surface-adjoining channel region of the first conductivity type in the epitaxial layer, a surface-adjoining source region of the second conductivity type in the channel region, and a surface-adjoining drain contact region of the second conductivity type in the epitaxial layer and spaced apart from the channel region. An insulating layer is provided on the surface layer and covers at least that portion of the channel region located between the source and drain. A gate electrode is provided on the insulating layer, over a portion of the channel region between the source and drain and is electrically isolated from the surface layer, while source and drain electrodes are connected respectively to the source and drain regions of the transistor. Such prior-art high-voltage DMOS transistors have a relatively thick surface layer (typically an epitaxial layer), in the order of about 25–30 microns for a breakdown voltage of about 250 V, as indicated in the Pocha et al paper. Furthermore, the punchthrough and avalanche breakdown characteristics of these devices relative to their epitaxial layer thickness make them unsuitable for efficient use in applications requiring high voltages.

It has been found that the breakdown characteristics of high-voltage semiconductor devices can be improved using the REduced SURface Field (or RESURF) technique, as described in "High Voltage Thin Layer Devices (RESURF Devices)", "International Electronic Devices Meeting Technical Digest", December 1979, pages 238–240, by Appels et al, and U.S. Pat. No. 4,292,642 to Appels et al. Essentially, the improved breakdown characteristics of these RESURF devices are achieved by employing thinner but more highly doped epitaxial layers to reduce surface fields. As defined in my U.S. Pat. No. 4,300,150, the RESURF principle requires that appropriate values for the product of layer thickness and resistivity be selected. More particularly, the product of doping concentration and layer thickness for RESURF is defined in my prior patent as typically approximately 10^{12} atoms/cm^2, with a representative value of $1.8(10)^{12}$ atoms/cm^2 shown in the examples.

The RESURF technique was applied to lateral double-diffused MOS transistors, as reported in "Lateral DMOS Power Transistor Design", "IEEE Electron Device Letters", Vol. EDL-1, pages 51–53, April, 1980, by Colak et al and my U.S. Pat. No. 4,300,150, and the result was a substantial improvement in device characteristics. It should be understood that in high-voltage DMOS devices, there is always a trade-off between breakdown voltage, on-resistance and device size, with the goal being to increase the breakdown voltage level while maintaining a relatively low on-resistance in a relatively compact device. Using the prior art RESURF technique, and for reference assuming a constant breakdown voltage of about 400 volts, a very substantial improvement (e.g. decrease) in on-resistance may be obtained in a device of the same size as a conventional (thick epitaxial layer) DMOS device.

However, such prior art RESURF devices, with their thin epitaxial layers, are not suitable for use in source-follower applications or other circuit arrangements where both the source and drain are at a high potential with respect to the substrate. For such applications, these devices would require a substantially thicker epitaxial surface layer, thus negating a principal advantage of the RESURF technique and increasing device size and cost, or they would require a lower epitaxial doping level, which would increase on-resistance, again negating a principal advantage of the RESURF technique.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a lateral double-diffused MOS transistor which is suitable for use in source-follower applications or other circuit arrangements where both the source and drain are at a high potential with respect to the substrate.

It is a further object of the invention to provide a lateral double-diffused MOS transistor suitable for source-follower applications while maintaining the advantages of devices constructed using the RESURF technique.

In accordance with the invention, these objectives are achieved by a lateral double-diffused MOS transistor of the type described above, in which the single prior-art surface layer on the semiconductor substrate is replaced by a 3-layer configuration including a first semiconductor layer of the second conductivity type on the substrate, a second semiconductor layer of the first conductivity type on the first layer, and a third semiconductor surface layer of the second conductivity type on the second layer. This 3-layer configuration permits operation in the source-follower mode by preventing device breakdown when both the source and drain are operated at relatively high voltages with respect to the substrate.

In a further embodiment of the invention, a plurality of spaced-apart semiconductor zones of the second conductivity type are located within that portion of the second semiconductor layer extending from adjacent the channel region to beneath the drain contact region. These semiconductor zones may either be strip-shaped zones which extend continuously from adjacent the channel region to beneath the drain contact region or else each zone may include first and second subzones, with the first subzone located adjacent to the channel region and the second subzone spaced apart from the first subzone and located beneath the drain contact region of the device. These semiconductor zones serve to prevent the first semiconductor layer from floating by connecting it to the third semiconductor surface layer of the device, and also provide an additional RE-

SURF effect in the lateral direction, thus improving both breakdown voltage and device conductivity.

In another embodiment of the invention, device conductivity can be further improved by providing a second drain region and a further gate electrode, so that the second semiconductor layer can also contribute to device conductivity when the transistor is in the "on" state.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a vertical cross-sectional view of a lateral double-diffused MOS transistor in accordance with a first embodiment of the invention;

FIG. 2A is a plan view along the section line II—II of the transistor of FIG. 1;

FIG. 2B is a plan view of a lateral double-diffused MOS transistor in accordance with a second embodiment of the invention;

FIG. 2C is a plan view of a lateral double-diffused MOS transistor in accordance with a third embodiment of the invention; and

FIG. 3 is a vertical cross-sectional view of a lateral double-diffused MOS transistor in accordance with a fourth embodiment of the invention.

DETAILED DESCRIPTION

As noted above, conventional lateral double-diffused MOS transistors are not suitable for efficient use in source-follower circuits, because of the relatively thick epitaxial layers required to avoid punchthrough breakdown in the source-follower mode. This results in an unduly large and expensive-to-manufacture device. Furthermore, prior-art RESURF techniques, which permit the use of thinner epitaxial layers, result in devices which are unsuited for source-follower applications because of similar high-voltage breakdown problems. More specifically, in typical source-follower applications, the device substrate is normally grounded, while the drain, source and channel regions of the device experience high voltage levels in the "on" state when these devices are operated with high power supply voltages. Under such condition, conventional RESURF devices are subject to punchthrough breakdown (from channel to substrate) which precludes operation in the source-follower mode.

These prior-art problems are overcome in the present invention by a device such as that shown in FIG. 1, employing a triple-layer structure above the substrate. It should be noted that FIG. 1, as well as the remaining figures of the drawing, are not drawn to scale, and in particular the vertical dimensions are exaggerated for improved clarity. Additionally, like parts are designated with like reference numerals in the various figures, and semiconductor regions of the same conductivity type are shown hatched in the same direction.

In FIG. 1, a lateral double-diffused MOS transistor 10 has a semiconductor substrate 12 of a first conductivity type, here p-type, on which the device is constructed. A first semiconductor layer 14 of a second conductivity type opposite to that of the first, here n-type, is located on a first major surface 12*a* of the substrate, while a second semiconductor layer 16 of the first conductivity type is located on the first semiconductor layer. The basic layered construction of the device is completed by a third semiconductor surface layer 18 of the second conductivity type which is located on the second layer.

The lateral double-diffused MOS transistor of the invention is constructed within this layered structure by providing a first surface-adjoining channel region 20 of p-type material in the third layer, with a surface-adjoining source region 22 of n-type material in a portion of p-type region 20. A first surface-adjoining drain contact region 24 of n-type material is provided in the third layer 18 and is spaced apart from the first channel region, and a portion of the third semiconductor surface layer 18 between the drain contact region 24 and the first channel region 20 forms an extended drain region 24*a*. Similarly, that portion of the second layer extending from the channel region 20 to beneath the first drain contact region 24 forms an extended channel region.

An insulating layer 26 is provided on the surface of the transistor, over the third surface layer, and covers at least the portion of the first channel region 20 which is located between the source and the first drain regions. A first gate electrode 30 is provided on the insulating layer 26, over the previously-mentioned portion of the first channel region, and is electrically isolated from the third layer by the insulating layer 26. An electrical connection to the first drain contact region 24 is provided by a first drain electrode 32, while a source electrode 28 is provided to contact the source region 22, and this source electrode also serves to connect the first channel region 20 to the source region 22. The basic construction of the device is completed by a substrate electrode 34 on lower major surface 12*b* of the substrate 12.

The principal difference between the present invention and prior-art lateral double-diffused MOS transistors, such as FIG. 1 of my U.S. Pat. No. 4,300,150, lies in the presence of the second semiconductor layer 16, which in FIG. 1 forms a p-type extension of the channel region 20 between the n-type first and third semiconductor layers, and which extends from the channel region 20 to beneath the drain region 24, 24*a*. This configuration is in contrast to the prior art device shown in FIG. 1 of my prior patent, in which the area between the channel and drain is composed of a single n-type layer 12.

The three-layer configuration of my present invention affords several important design advantages, which permit the use of devices incorporating the present invention in source-follower circuits. In particular, by providing an extended channel in the form of second semiconductor layer 16, it is possible to increase the doping levels of the n-type first and third semiconductor layers to substantially avoid the channel-to-substrate punchthrough breakdown problem previously described. Ordinarily, such an increased doping level would be undesirable because it would reduce the drain-to-channel avalanche breakdown voltage of the device, but here, by adding the p-type second semiconductor layer, this undesirable decrease in avalanche breakdown voltage is substantially avoided. By redistributing the electrical field over a greater area of the device, the p-type second semiconductor layer utilizes the basic RESURF principle to reduce the localized magnitude of the electrical field adjacent the channel, and thus prevents avalanche breakdown in this region when higher doping levels are used in the third, and particularly the first, semiconductor layers in order to prevent punchthrough during operation in the source-follower mode. Thus, the present invention results in a device which is particularly suitable for high-voltage operation in the source-follower mode due to its improved punchthrough and avalanche breakdown characteristics.

Furthermore, in accordance with basic RESURF principles, the three semiconductor layers are not only more highly-doped than in conventional devices, but are also substantially thinner, thus resulting in a smaller, less expensive and easier-to-manufacture device. Thus, while the total thickness of all three semiconductor layers (i.e. the total thickness between insulating layer 26 and the upper surface 12a of the substrate) may typically be about 6 microns in the present invention for a device capable of operating at 400 volts, the prior-art MOS structure of Pocha et al, described above, requires an epitaxial layer thickness of greater than 23 microns in order to achieve a punchthrough breakdown voltage of only 200 volts. In addition, the relatively high doping levels of the semiconductor layers in the present invention provide improved normalized "on" resistance despite the use of relatively thin semiconductor layers. Thus, the present invention serves to improve both breakdown voltage and normalized "on" resistance, thereby permitting effective and efficient operation in the source-follower mode.

While the configuration of the present invention can be advantageously used in various device constructions, the following table of approximate values will illustrate the configuration of a typical device having a breakdown voltage of about 400 volts:

REGION (Ref. No.)	TYPE	TYPICAL DOPING	TYPICAL THICKNESS
First semiconductor layer (14)	n+	10^{16} donors/cm^3	2 microns
Second semiconductor layer (16)	p+	10^{16} acceptors/cm^3	2 microns
Third semiconductor layer (18)	n+	10^{16} donors/cm^3	2 microns
Source (22)	n++	10^{19}–10^{20} donors/cm^3	2 microns
Drain	n++	10^{19}–10^{20} donors/cm^3	2 microns
Contact (24)			
Channel (20)	p++	10^{17}–10^{20} acceptors/cm^3	4 microns
Substrate (12)	p–	10^{14}–10^{15} acceptors/cm^3	—

As can be seen from the above table, the product of doping concentration and layer thickness for the first, second and third layers is typically about $2(10)^{12}$ atoms/cm^2, in accordance with the RESURF principle.

A plan view of the device of FIG. 1 along the section line II—II is shown in FIG. 2A. This plan view shows a horizontal section of the p-type second semiconductor layer 16, as well as a portion of the more highly-doped channel region 20 which extends into the second semiconductor layer beneath the source. Due to the substantially continuous nature of this intermediate p-type layer between the upper (third) and lower (first) semiconductor layers, the lower n-type semiconductor layer does not conduct a portion of the total device current in the "on" state because layer 14 is isolated from the current-carrying path due to the intervening second semiconductor layer 16. However, substantial further reduction in normalized "on" resistance could be attained if the first semiconductor layer 16 of FIG. 2A were to be used as an additional current path. Two alternate embodiments for accomplishing this function are shown in FIGS. 2B and 2C.

In these embodiments, a plurality of spaced-apart semiconductor zones 16c, 16d of the second conductivity type (here n-type) are located within that portion of the second semiconductor layer 16 extending from adjacent the channel region 20 to beneath the drain contact region 24. In FIG. 2B, these semiconductor zones are formed from strip-shaped zones 16c which extend continuously from adjacent the channel region to beneath the drain contact region, while in FIG. 2C, each spaced-apart semiconductor zone is formed from a first sub-zone 16d located adjacent the channel region and a second sub-zone 16d' which is spaced apart from the first sub-zone and is located beneath the drain contact region. These spaced-apart semiconductor zones 16c, 16d and 16d' are n-type zones having a typical doping level of about 10^{16} donors/cm^3. In FIG. 2B, the lateral extent of the semiconductor zones 16c is shown by reference numerals 16a and 16b to denote the left and right edges, respectively, of the zones. In FIG. 1, dotted lines are used to show where these left and right edges would appear in a cross-section along the line I—I of FIG. 2B if these semiconductor zones were to be incorporated into the device of FIG. 1. As shown in FIG. 1, the semiconductor zones extend in the vertical direction from the third semiconductor layer 18 down to the first semiconductor layer 14.

By means of these semiconductor zones, a connection is formed between the upper (third) and lower (first) semiconductor layers, so that the first semiconductor layer is no longer floating, and can contribute to device conductivity in the "on" state, thus lowering normalized "on" resistance. In fact, normalized "on" resistance will be reduced by a factor of about 2 by including these semiconductor zones in the embodiment of FIG. 1. Additionally, by preventing the lower (first) semiconductor layer from floating by connecting it to the uppermost (third) semiconductor layer, an additional advantage is obtained in that the avalanche breakdown voltage of the device will be increased. Furthermore, with these zones, the critical nature of the upper (third) semiconductor layer decreases, so that it can be made thinner.

An additional embodiment of the invention, in which device conductivity is further improved, is shown in FIG. 3. This device differs from the device shown in FIG. 1 basically in that the single gate and drain structure of FIG. 1 is replaced by a modified dual-gate/dual-drain structure. More particularly, lateral double-diffused MOS transistor 11 includes a second surface-adjoining drain end region 40 of p-type material, as well as a second surface-adjoining channel region 36 of n-type material which is controlled by a further gate electrode 46 (G2) located over the second channel region. The embodiment of FIG. 3 also differs from the previously-described embodiment of FIG. 1 in that the original drain contact region 24 (hereinafter referred to as the first drain contact region for clarity) now includes a p-type surface region 38 within the n-type region 36, so that region 36 now also serves as a second surface-adjoining channel region for the new portion (on its right side), while the p-type zone 38 serves as a further surface-adjoining source region for the new portion of the device. A first drain electrode 44 contacts both source region 38 and region 36, and now serves as both a drain electrode (D1) for the original portion of the device and as a source electrode (S2) for the new portion. The purpose of this more complex dual-gate/dual-drain structure is to enhance device conductivity in the "on" state by enabling the second p-type semiconductor layer 16 to also contribute to device conductivity by conducting holes from region 38, through the second

channel region 36, the second drain end region 40 and the second semiconductor layer 16 back to source region 22. Electrode 28, which contacts both regions 20 and 22, now serves as both a source electrode (S1) for the original portion of the device and as a drain electrode (D2) for the new portion.

Yet a further improvement in normalized "on" resistance may be achieved by combining the dual-gate/dual-drain structure of FIG. 3 with the spaced-apart semiconductor zones 16c or 16d/d' of FIG. 2B or 2C. In this manner all three semiconductor layers will contribute to device conductivity, thus achieving optimum normalized "on" resistance.

Thus, by using a unique triple-layer construction, the present invention provides a lateral double-diffused MOS transistor which is capable of operating at high voltages in the source-follower mode, while at the same time providing a low normalized "on" resistance in a vertically compact and easily manufactured structure.

Finally, while the invention has been particularly shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made without departing from the spirit and scope of the invention.

I claim:

1. A lateral double-diffused MOS transistor, which comprises:

a semiconductor substrate of a first conductivity type;

a first semiconductor layer of a second conductivity type opposite to that of the first on a first major surface of said substrate;

a second semiconductor layer of said first conductivity type on said first layer;

a third semiconductor surface layer of said second conductivity type on said second layer, the product of the net doping concentration and the thickness of said first, second and third semiconductor layers each being selected to accordance with the RESURF principle such that the product of doping concentration and layer thickness is typically approximately 10^{12} atoms/cm^2;

a first surface-adjoining channel region of said first conductivity type in said third layer and connected to said second semiconductor layer;

a surface-adjoining source region of said second conductivity type in said channel region;

a first surface-adjoining drain contact region of said second conductivity type in said third layer and spaced apart from said first channel region;

an extended drain region formed from a portion of said third layer between said first drain contact region and said first channel region;

an insulating layer on the surface of said transistor and covering at least that portion of the first surface-adjoining channel region located between said source and said extended drain regions;

a first gate electrode on said insulating layer, over said portion of the first channel region and electrically isolated from said third layer; and

source and first drain electrodes connected respectively to the source and first drain contact regions of the transistor.

2. A lateral double-diffused MOS transistor as in claim 1, wherein the doping level of said second layer is higher than that of said substrate, the doping level of said first channel region is higher than that of said second layer, and the doping level of said source and first drain contact regions is higher than the doping level of said first and third layers.

3. A lateral double-diffused MOS transistor as in claim 2, wherein said source electrode electrically connects said source and first channel regions together, and further comprising a substrate electrode on a second major surface of said substrate opposite said first major surface.

4. A lateral double-diffused MOS transistor as in claim 1, further comprising a plurality of spaced-apart semiconductor zones of said second conductivity type located in that portion of said second semiconductor layer extending laterally from adjacent said first channel region to beneath said first drain contact region, said semiconductor zones extending vertically from said first semiconductor layer to said third semiconductor layer.

5. A lateral double-diffused MOS transistor as claimed in claim 4, wherein said spaced-apart zones comprise strip-shaped zones extending continuously from adjacent said first channel region to beneath said first drain contact region.

6. A lateral double-diffused MOS transistor as claimed in claim 4, wherein each of said spaced-apart zones comprises a first subzone located adjacent said first channel region and a second subzone, spaced apart from said first subzone and located beneath said first drain contact region.

7. A lateral double-diffused MOS transistor as claimed in claim 4, wherein said spaced-apart semiconductor zones comprise n-type zones having a doping level of about 10^{16} donors/cm^3.

8. A lateral double-diffused MOS transistor as in claim 1, further comprising a second surface-adjoining drain end region of said first conductivity type in said third layer, extending down to said first layer, and electrically isolated from said first drain contact region by a p-n junction, a second surface-adjoining channel region of said second conductivity type between said first drain contact region and said second drain end region, said insulating layer on the surface of said transistor further covering that portion of the second surface-adjoining channel region located between said drain regions, a further surface-adjoining source region of said first conductivity type in said second surface-adjoining channel region and connected to said first drain electrode, and a further gate electrode on said insulating layer, over said portion of the second channel region and electrically isolated from said third layer.

9. A lateral double-diffused MOS transistor as in claim 8, further comprising a plurality of spaced-apart semiconductor zones of said second conductivity type located in that portion of said second semiconductor layer extending laterally from adjacent said first channel region to at least beneath said first drain contact region, said semiconductor zones extending vertically from said first semiconductor layer to said third semiconductor layer.

10. A lateral double-diffused MOS transistor as claimed in claim 9, wherein said spaced-apart zones comprise strip-shaped zones extending continuously from adjacent said first channel region to at least beneath said first drain contact region.

11. A lateral double-diffused MOS transistor as claimed in claim 9, wherein each of said spaced-apart zones comprises a first subzone located adjacent said first channel region and a second subzone, spaced apart

from said first subzone and located beneath said first drain contact region.

12. A lateral double-diffused MOS transistor as in claim 1, wherein said first and third semiconductor layers comprise n-type layers having a doping level of about 10^{16} donors/cm^3, and a thickness of about 2 microns, and said second semiconductor layer comprises a p-type layer having a doping level of about 10^{16} acceptors/cm^3 and a thickness of about 2 microns.

* * * * *

DX 90

REDACTED